Regulation: R23

23EE51-ELECTRICAL & ELECTRONICS ENGINEERING WORKSHOP

LABORATORY MANUAL

(Electrical and Electronics Engineering)

LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS) MYLAVARAM-521230

PART A : ELECTRICAL ENGINEERING LAB

Course Objectives:

To impart knowledge on the fundamental laws & theorems of electrical circuits, functions of electrical machines and energy calculations.

Course Outcomes:

After competition of this course, the student will be able to
CO1. Measure voltage, current and power in an electrical circuit. (L3)
CO2. Measure of Resistance using Wheat stone bridge (L4)
CO3. Discover critical field resistance and critical speed of DC shunt generators. (L4)
CO4. Investigate the effect of reactive power and power factor in electrical loads. (L5)

List of experiments:

1. Verification of KCL and KVL
2. Verification of Superposition theorem
3. Measurement of Resistance using Wheat stone bridge
4. Magnetization Characteristics of DC shunt Generator
5. Measurement of Power and Power factor using Single-phase wattmeter
6. Measurement of Earth Resistance using Megger
7. Calculation of Electrical Energy for Domestic Premises

Experiment No : 1 Date :

VERIFICATION OF KCL AND KVL

AIM : To Verify Kirchhoff's current and voltage laws for the given circuit.

APPARATUS REQUIRED :

S.NO.	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1.	Regulated Power Supply (RPS)	(0 – 30) V	1
2.	Rheostat	50 Ω/5 A	1
		25 Ω/5 A	1
		18 Ω/5 A	1
3.	Ammeter	(0-1) A , MC	3
4.	Voltmeter	(0-10) V, MC	3
5.	Connecting Wires	--	Required

THEORY :

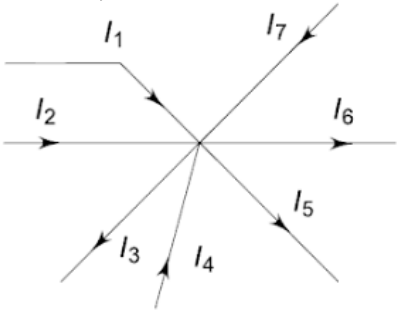
KIRCHHOFF'S CURRENT LAW (KVL)

Statement:

Kirchhoff's current law states that the sure of the currents entering into any node is equal to the sum of the currents leaving that node.

The node may be an interconnection of two or more branches. In any parallel circuit, the node is a junction point of two or more branches. The total current entering into a node is equal to the current leaving that node.

In general, sum of the currents entering any point or node or junction equal to sum of the currents leaving from that point or node or junction as shown in Fig.



$$I_1 + I_2 + I_4 + I_7 = I_3 + I_5 + I_6$$

If all of the terms on the right side are brought over to the left side, their signs change to negative and a zero is left on the right side, i.e.

$$I_1 + I_2 + I_4 + I_7 - I_3 - I_5 - I_6 = 0$$

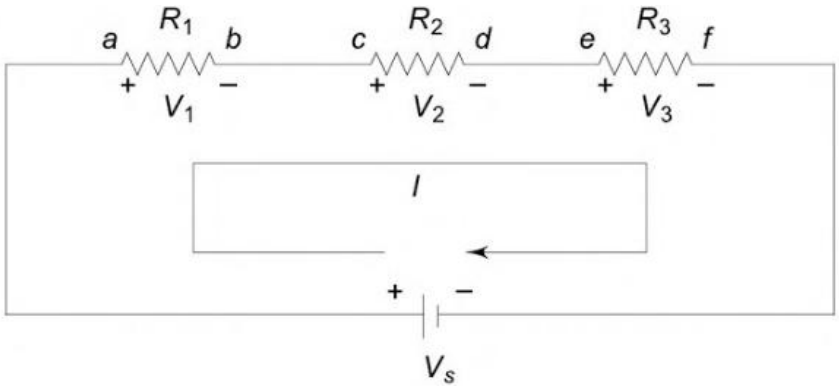
This means that the algebraic sum of all the currents meeting at a junction is equal to zero.

KIRCHHOFF'S VOLTAGE LAW (KVL)

Statement:

Kirchhoff's voltage law states that the algebraic sum of all branch voltages around any closed path in a circuit is always zero at all instants of time.

When the current passes through a resistor, there is a loss of energy and, therefore, a voltage drop. In any element, the current always flows from higher potential to lower potential. Consider the circuit in Fig. It is customary to take the direction of current I as indicated in the figure, i.e. it leaves the positive terminal of the voltage source and enters into the negative terminal.

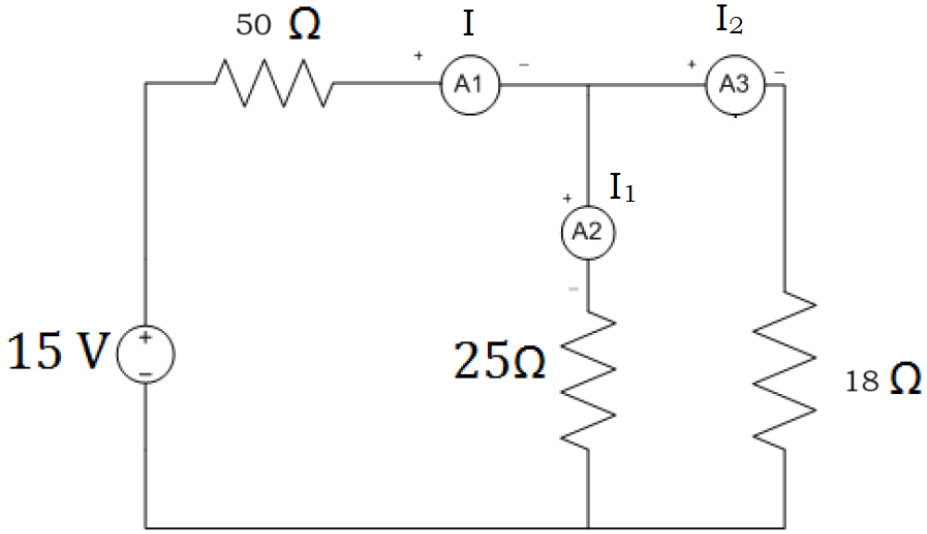


As the current passes through the circuit, the sum of the voltage drop around the loop is equal to the total voltage in that loop. Here the polarities are attributed to the resistors to indicate that the voltages at points a, c and e are more than the voltages at b, d and f, respectively, as the current passes from a to f.

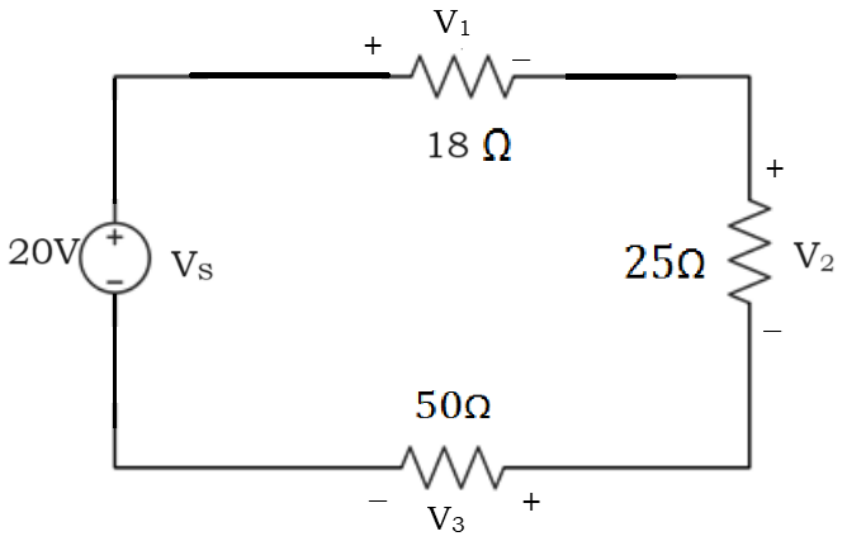
$$\therefore \quad V_s = V_1 + V_2 + V_3$$

CIRCUIT DIAGRAM:

KCL:



KVL :



PROCEDURE :

1. Connect the circuit diagrams as shown in the fig. for KCL and KVL.
2. Using RPS, apply the given supply voltage.
3. For KCL, measure the ammeter readings.
4. For KVL, measure the voltmeter readings.
5. Tabulate the values of voltages and currents of KVL and KCL.
6. Verify KCL as $I=I_1+I_2$ and KVL as $V_S = V_1 + V_2 + V_3$.

THEORETICAL CALCULATIONS :

TABULAR COLUMNS :

PARAMETERS	KVL				KCL		
	V_S	**V_1**	**V_2**	**V_3**	**I**	**I_1**	**I_2**
THEORETICAL							
PRACTICAL							

PRECAUTIONS :

1. Check the connections before switching ON the supply.
2. The terminals of the rheostat should be properly connected.
3. Disconnect the connections properly after the completion of experiment.
4. Measure the readings accurately without parallax error.

RESULT :

The KVL and KCL for the given circuit are verified theoretically and practically.

Viva Questions:

1) What is Current Divider Rule ?
2) What is Voltage Divider Rule?
3) What is Current?
4) Could you measure Voltage in series?
5) What is Kirchoff‟s Current Law (KCL)?
6) Define Voltage.
7) Define Ohm‟s Law for A.C ?
8) What do you mean by dependent and independent voltage sources?
9) How does a capacitor store an electrical charge?
10) Could you measure current in parallel?

Experiment No : 2 Date :

VERIFICATION OF SUPERPOSITION THEOREM

AIM : To verify the superposition theorem by determining the current flowing through the resistance R.

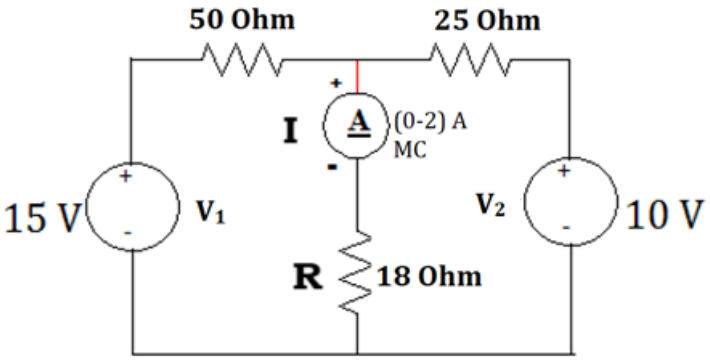
APPARATUS REQUIRED :

S.NO.	NAME OF THE EQUIPMENT	RANGE	QUANTITY
1.	Regulated Power Supply (RPS)	(0 – 30) V	1
2.	Rheostat	50 Ω/5 A	1
		25 Ω/5 A	1
		18 Ω/5 A	1
3.	Ammeter	(0-2) A , MC	1
4.	Connecting Wires	--	Required

THEORY :

The superposition theorem states that in any linear network containing two or more sources, the response in any element is equal to the algebraic sum of the responses caused by individual sources acting alone, while the other sources are non-operative; that is, while considering the effect of individual sources, other ideal voltage sources and ideal current sources in the network are replaced by short circuit and open circuit across their terminals respectively. This theorem is valid only for linear systems.

CIRCUIT DIAGRAM :



(a)

PROCEDURE :

1. Connect the circuit as shown in the Circuit diagram (a).
2. Switch ON the supply voltage (DC) and apply V_1 and V_2.
3. Note down the Ammeter reading as I.
4. Make V_1= 0 and apply V_2, note down the ammeter reading as I_1.
5. Make V_2= 0 and apply V_1, note down the ammeter reading as I_2.
6. Verify the condition $I = I_1 + I_2$

THEORETICAL CALCULATIONS :

TABULAR COLUMNS :

S.NO.	Parameter	V_1 = 15V, V_2 = 10V	V_1 = 0V, V_2 = 10V	V_1 = 15V, V_2 = 0V
1.	Current through 18 Ohm (Theoretical)			
2.	Current through 18 Ohm (Practical)			

PRECAUTIONS :

1. Check the connections before switching ON the supply.
2. The terminals of the rheostat should be properly connected.
3. Disconnect the connections properly after the completion of experiment.
4. Measure the readings accurately without parallax error.

RESULT :

The superposition theorem is verified for the given circuit theoretically and practically.

Experiment No : 3 Date :

MEASUREMENT OF RESISTANCE USING WHEATSTONE BRIDGE

Aim:

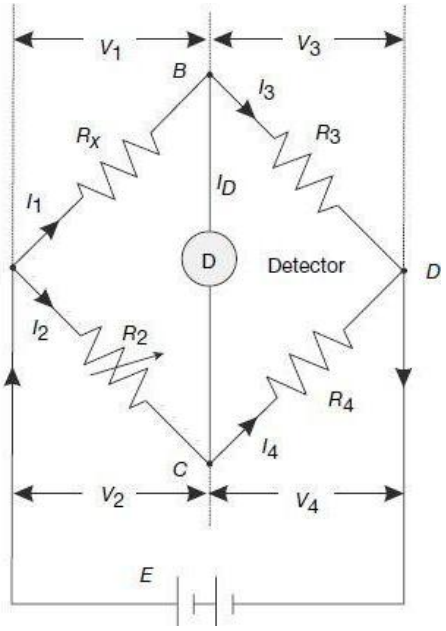
To measure the unknown medium resistance using Wheatstone's bridge.

Apparatus:

S.NO.	Name	Range	Type	Quantity
1	Wheatstone's bridge trainer kit	--	--	1
2	Connecting wires	--	--	Required

Theory:

The Wheatstone bridge is the most commonly used circuit for measurement of medium range resistances. The Wheatstone bridge consists of four resistance arms, together with a battery (voltage source) and a galvanometer (null detector). The circuit is shown in Figure.



In the bridge circuit, R3 and R4 are two fixed known resistances, R2 is a known variable resistance and RX is the unknown resistance to be measured. Under operating conditions, current ID through the galvanometer will depend on the difference in potential between nodes B and C. A bridge balance condition is achieved by varying the resistance R2 and checking whether the galvanometer pointer is resting at its zero position. At balance, no current flows through the galvanometer. This means that at balance, potentials at nodes B and C are equal.

The unknown resistance can be calculated as

$$R_X = R_2 \times \frac{R_3}{R_4}$$

Procedure:

1) Connect the fixed resistances on the trainer kit.

2) Switch ON the supply.

3) Vary the value of variable resistance upto the galvanometer shows zero value.

4) Hence calculate the value of unknown resistance by using the formula.

$$R_X = R_2 \times \frac{R_3}{R_4}$$

TABULAR COLUMN:

S.NO.	R_2	R_3	R_4	R_X
1.				
2.				
3.				
4.				

Precautions:

1) Vary the value of variable resistance with different ranges.

2) Switch OFF the trainer kit after completion of experiment.

Result:

The unknown resistance is calculated using Wheatstone's bridge.

Experiment No : 4 Date :

MAGNETIZATION CHARACTERISTICS OF D.C. SHUNT GENERATOR

AIM:- To draw the open circuit or magnetization characteristics and to determine the critical resistance and critical speed of a DC Shunt generator.

APPARATUS:

S.no.	Name	Range	Type	Quantity
1.	Voltmeter	0-300V	MC	1 No.
2.	Ammeter	0-2A	MC	1 No.
3.	Rheostat	18Ω/ 12A	MC	1 No.
4.	Rheostat	360Ω/ 1.2A	MC	2 Nos.
5.	Connecting wires			Required

THEORY:

Magnetization Curve:

The graph between the field current and no load induced emf is called the magnetization characteristics of a machine. This is same as B-H curve of the material used for the pole construction. Due to residual magnetism in the poles, some emf is generated even when I_f=0. Hence the curve starts a little way up. The slight curvature at lower end is due to magnetic inertia. It seen that the first part of the curve is practically straight. This is due fact that at lower flux densities, reluctance of the iron path being negligible, total reluctance is given air gap reluctance which is constant. Hence, the flux and consequently, the generated emf is directly proportional to the field current. However at higher flux densities where permeability is small, iron path reluctance becomes appreciable and straight relation between E and I_f no longer holds good. In other words saturation of poles starts.

Critical Resistance(R_C):

It is defined as the amount of field resistance required to generate emf in the armature winding. (or) The critical field resistance is defined as the field resistance of the generator which holds the rated voltage of it. (or) It is the value of field resistance beyond which the generator fails to build up the voltage if there is a further increase in the field resistance.

Critical Speed(N_C):

Critical speed is defined as the speed at which the given shunt field resistance is equal to the critical resistance. It is the speed at which the shunt generator just fails to build up its voltage without any external resistance in the field circuit. It is denoted by Nc.

PROCEDURE:

1) All the connections are done as per the circuit diagram.

2) Before giving the supply to the motor, armature rheostat is kept at maximum resistance position and field rheostat is kept at minimum resistance position and filed rheostat of generator is kept at maximum resistance position.

3) Supply is given to the motor.

4) Start the motor with the help of 3-point starter.

5) Speed of the motor is adjusted to rated value by using armature and field rheostats of motor circuit.

6) Ammeter and voltmeter reading are noted.

7) By varying the field rheostat of generator, the readings of ammeter and voltmeter are noted for each step of variation of rheostat. At each step of variation the speed should be kept constant.

8) The meter readings are noted until the generated voltage is just above the rated voltage.

9) After plotting the magnetization characteristics draw a tangent line to its initial portion, which passes through the origin.

10) Calculate the slope of this tangent line, which gives the critical field resistance (Rc) at the rated speed of the generator.

11) Draw the designed field resistance line (Rf)

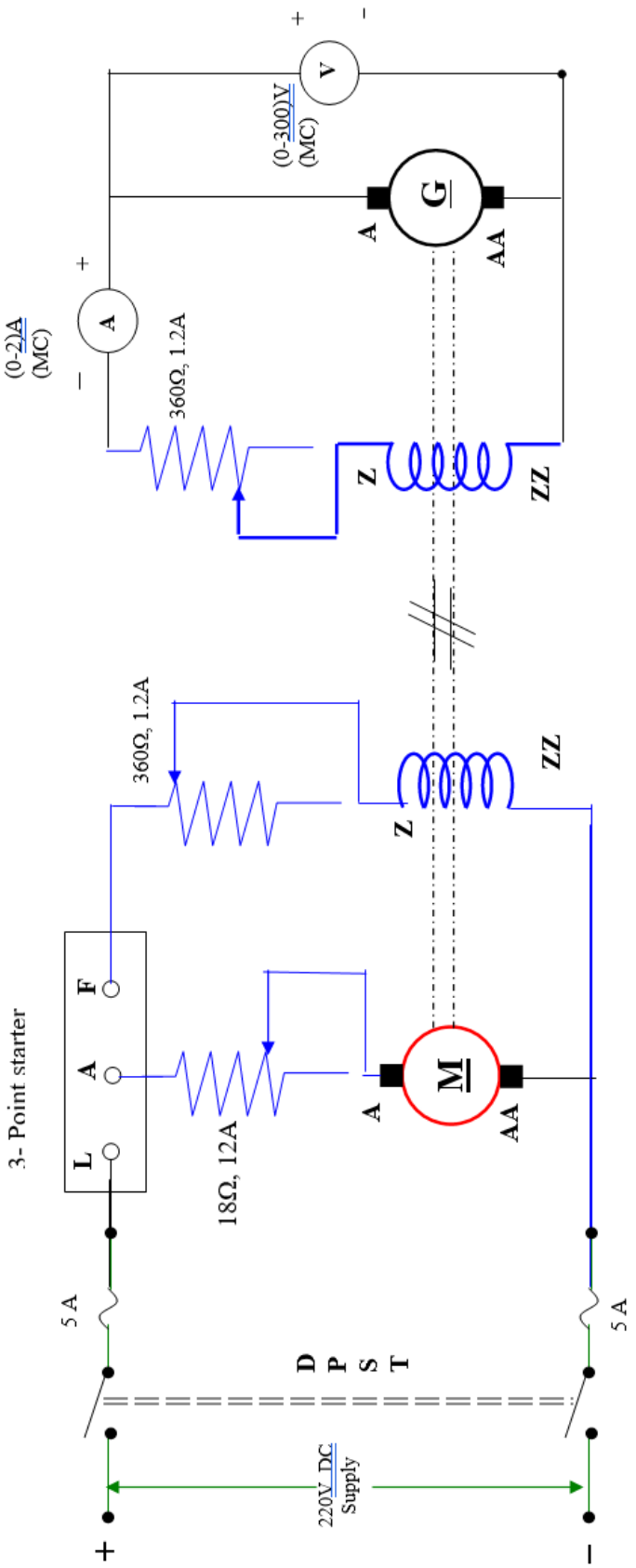
12) Draw a line parallel to y-axis, which cuts the Rf line and Rc line with in the linear portion of the magnetization characteristics.

13) Take the generated emf values corresponding to points of intersection of the line.

14) Calculate the critical speed using the formula.

$$N_C = \frac{E_1}{E_2} \times N_{rated}$$

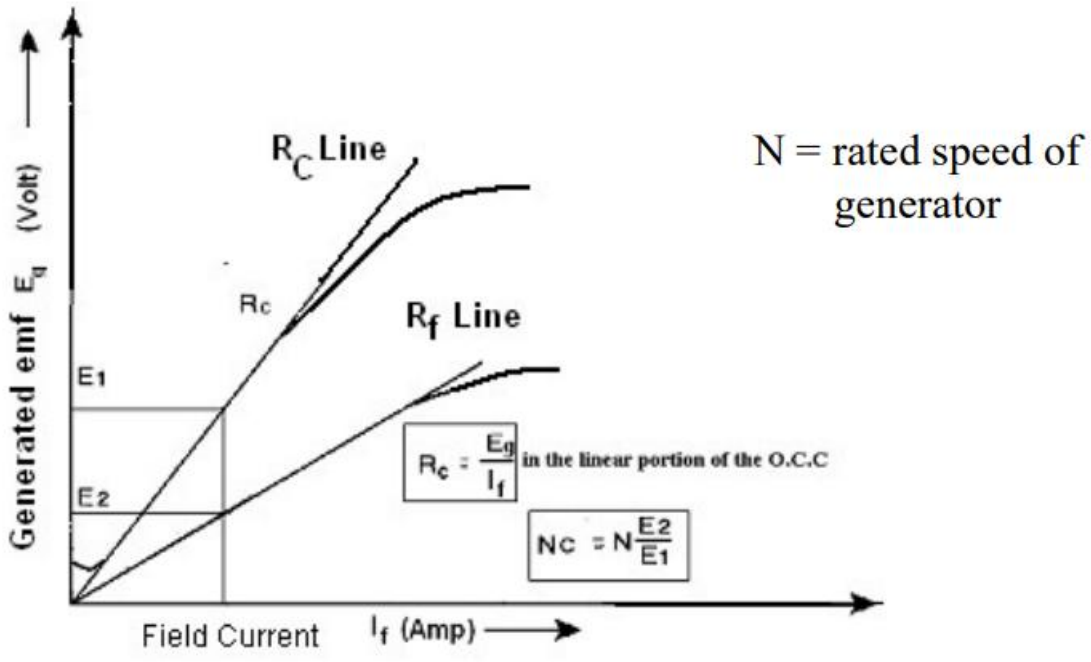
CIRCUIT DIAGRAM



OBSERVATIONS:

S.No.	Generated voltage (Volts)	Field current(Amps)

MODEL CHARACTERISTICS:



PRECAUTIONS:

1) The field rheostat of motor should be in minimum resistance position at the time of starting to start the machine from minimum speed.
2. The field rheostat of generator should be in maximum resistance position at the time of starting and stopping the machine.
3. Residual voltage should be taken under no field current.
4. The characteristics should be drawn at constant rated speed by adjusting the drive unit or motor filed resistance as required.

RESULT:

The critical resistance and critical speed are determined from the magnetization characteristics of DC shunt generator.

Viva Questions:

1. What is critical field resistance?
2. What are the conditions to build up e.m.f ?
3. What is critical speed?
4. Does voltage will be developed at zero field current?
5. What are the reasons for failure of building up e.m.f in a DC generator?
6. What are different types of DC generators?
7. What is meant by prime mover?
8. Why Rsh > Ra in DC shunt machine.
9. How to draw OCC curve?
10. How to find critical speed?

Experiment No : 5 Date :

MEASUREMENT OF POWER AND POWER FACTOR USING SINGLE-PHASE WATTMETER

Aim: To measure the power and power factor of series RL load using single-phase wattmeter.

Objective:

(i) To connect a wattmeter and power factor meter in a single phase circuit for measurement of power and power factor of load.

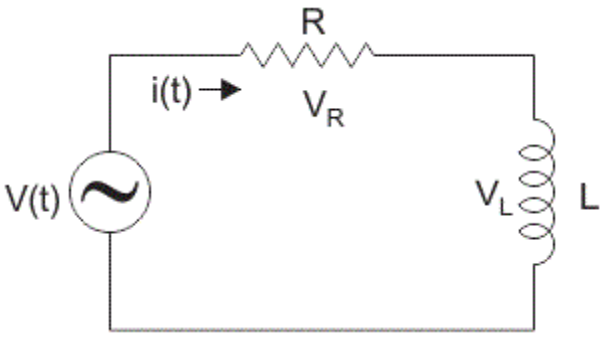
(ii) To verify relation $P = VICOS\emptyset$, from actual measurement of power, voltage, current and power factor.

Apparatus:

S.NO.	Name	Range	Type	Quantity
1	Dimmerstat or Variac	0-230V	1-Φ	1
1	Voltmeter	0-100V	MI	1
2	Ammeter	0-5A	MI	1
3	Wattmeter	300V, 5A	UPF	1
4	Power Factor Meter	300V, 5A		1
5	Rheostat	100 Ω,5A		1
6	Connecting wires			Required

Theory:

Series RL Circuit:

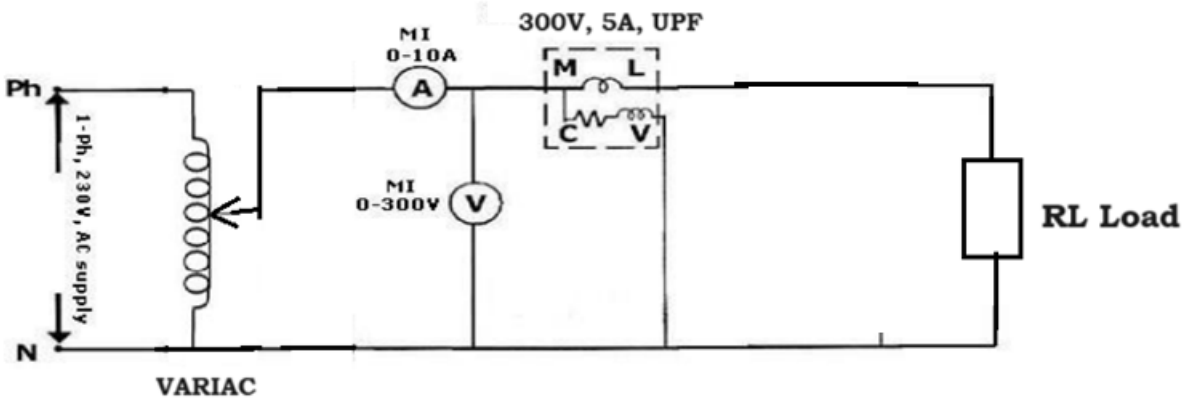


Consider a simple RL circuit in which resistor, R and inductor, L are connected in series with a voltage supply of V volts. Let us think the current flowing in the circuit is I (amp) and current through resistor and inductor is IR and IL respectively. Since both resistance and inductor are connected in series, so the current in both the elements and the circuit remains the same. i.e $I_R = I_L = I$. Let V_R and V_L be the voltage drop across resistor and inductor.

Applying Kirchhoff voltage law (i.e sum of voltage drop must be equal to apply voltage) to this circuit we get,

$$V = V_R + V_L$$

Circuit Diagram:



Procedure:

1. Make connections as per the circuit diagram.
2. Switch on the a.c supply through a variac fix up to the rated input voltage.
3. Increase the load current by variac and note down wattmeter, power factor meters, voltmeter and ammeter readings.
4. Calculate the power and power factor of single phase RL load.
5. Tabulate the readings of voltmeter, ammeter, wattmeter and power factor meter.

Observations:

Tabulation for RL-Load: R=100 Ohms.

S.No.	L	V	I	Wattmeter reading(W)	Power Factor $Cos\Phi = W/VI$
1.	50mH				
2.	100mH				
3.	125mH				

Precautions:

1. Loose connections should be avoided.
2. Meter reading should not exceed beyond their rating.
3. Take readings carefully.

Result: The power and power factor are measured for RL load using single phase wattmeter.

VIVA-VOICE

1. How the power factor of a single phase circuit is measured?
2. What is principle of power factor meter?
3. What are the different types of power factor meters?
4. Why is moving iron power factor meter generally used?
5. Why moving iron PF meters less accurate than dynamometer type?
6. What is power factor?
7. Give expression for the PF?
8. What is synchroscope and where it is used?
9. What is crossed coil PF meter?
10. What is instrument for speed measurements?

Experiment No : 6 Date :

MEASUREMENT OF EARTH RESISTANCE USING MEGGER

AIM: To measure the earth resistance using Megger.

Apparatus:

S.NO.	Name	Range	Type	Quantity
1	Megger Kit	--	Digital	1
2	Multimeter	--	Digital	1
3	Copper Rods	--	--	3
4	Connecting wires			Required

Theory:

Digital Earth resistance tester is direct replacement of the convention hand generator type tester. It is designed for measurement of the resistance of earth used in power circuits. Telecommunication, Railway electrification, domestic & industrial electrical installation, lighting protection installation and various other electrical systems. The instrument perform equally well in Terrain where the conductivity of the soil is low e.g. in mountaineous areas and in places where powerful stray earth current exist.

The instrument is specially designed for making straight forward and approximate soil investigation of the kind needed in agricultural, geological research and in planning of large civil engineering projects such as tunnels, Dams, Drainage, Sewerage schemes, Tube-Railways etc.

The tester measures directly the resistance of the earth and also measure the ground resistivity. The sturdy, elegant and compact body makes the instrument portable, easy-to-use-Hand-held instrument.

Four Terminals marked as E1, P1, E2 & P2.

The instrument is powered by rechargeable Nicd Cells. Low battery (LO BAT or Δ sign) indication appears on LCD indicates that the battery goes down, which can be recharged by connecting mains A.C. supply through charging chord provided with the instrument.

Operating Principle:

The principle used in measuring the earth resistance is based on simple ohm's law. Four Electrodes A,B,C,D are buried in the earth, the resistance of which is to be tested at a distance of 20 meters from each other as shown in Fig. 1

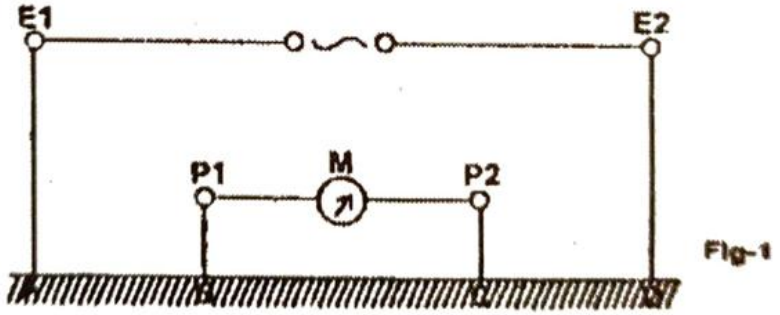


Fig-1

A.C. signal is applied to electrodes A and D and voltage developed across electrodes B and C due to flow of current through the earth is measured by ammeter M. If current is constant, the voltage measured will be directly proportional to the earth resistance.

Principle of Measurement:

To find out Resistance of earth connection, three terminal method is to be used.

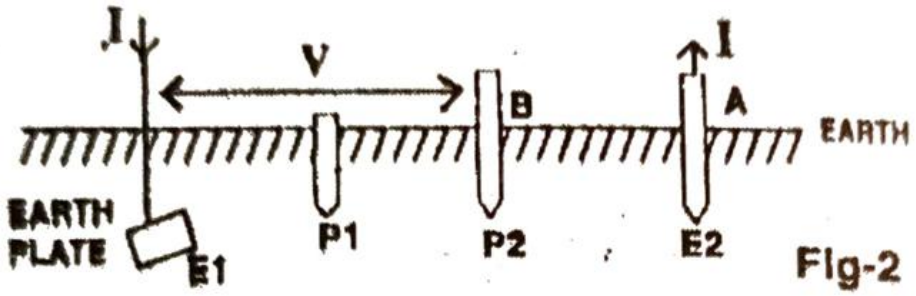


Fig-2

A current is passed through the EARTH PLATE to an auxiliary electrode A in the earth at a distance away from the earth plate.

A second auxiliary electrode B is inserted between EARTH PLATE AND "A", and the potential difference V between E and B is measured for a given current I so that the resistance of earth connection is V/I. The placing of the auxiliary electrode is however important. Following is the curve which given a plot of distance of B from E versus measured resistance.

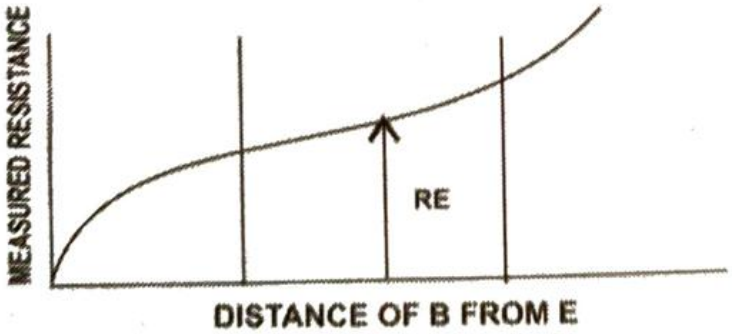


Fig-3

When earthing resistance is low, the spacing between the earth plate and auxiliary electrode may be 20 to 30 meters. The exact value can be decided by actual experiment.

If the instrument is to be used for above application, Terminals E1 & P1 is to be shorted (as shown in Fig. 4 below)

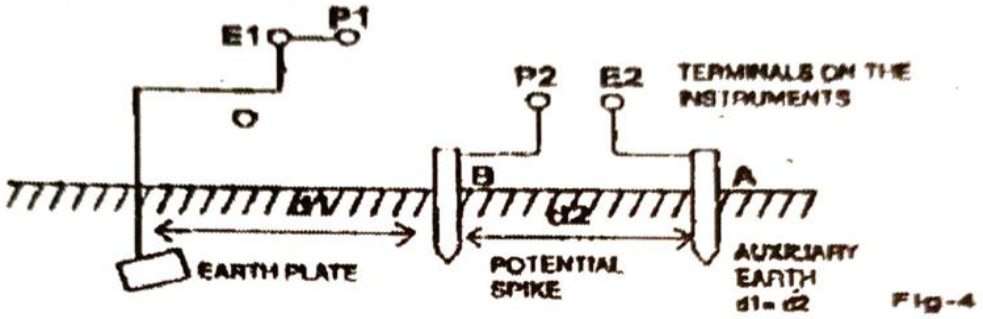


Fig-4

Terminal P2 has to be connected to Potential spike and terminal E2 to the auxiliary Earth as shown in Fig. Under this condition meter wil give the resistance of the earthing connection and the earth. To avoid error due to the wire resistances, first short the wires and note down the meter reading. Then connect the wires to the different electrodes as explained above, This reading minus the reading with wire shorted will give actual valued of resistance. The distance d1 and d2 may range from 20 to 30 meters depending upon the soil.

PROCEDURE:

MEASUREMENT OF EARTH RESISTANCE :

To measure Earth resistance with digital earth tester, it should be used as three terminal type. For that Terming E1 & P1 is to be shorter and connected to the Earth connection whose resistance has to be found (As shown in Fig. 5)

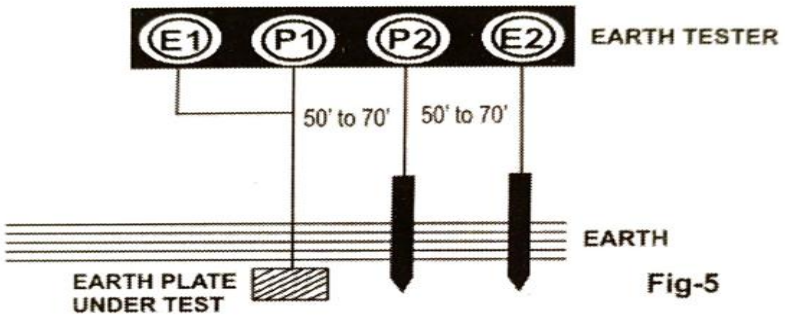


Fig-5

Connect as per Fig. 5 and take the reading by pressing the Test switch. Note down the reading displayed on the LCD of the instrument.

MEASUREMENT OF EARTH RESISTIVITY :

To find out the earth Resistivity for preferred positioning and depth of proposed electrode system, four terminals method is to be used. Connect the instrument terminals as per Fig6.

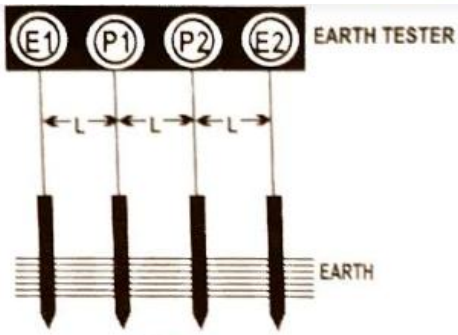


Fig-6

All the four spikes to be buried in one straight line and distance between them to be kept same.

The value of "L" may be kept between 50' to 70'

Take the reading by pressing the Test switch (Taking Care of Range Factor) Observed value is in ohms.

The value of Earth Resistivity " ρ " may be obtained from the following formula.

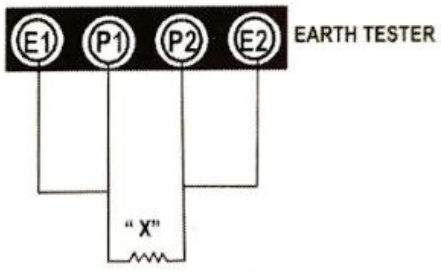
$$\rho = 2 \pi LR \text{ ohms-cms.}$$

Where R = Value of Earth Resistance measured in ohms.
L = Distance between spikes in cm.
π = 3.14
ρ = Earth's Resistivity in ohms - cms.

MEASUREMENT OF RESISTANCE

(Non inductive or Non-Capacitive)

Connect the unknown Resistance 'X' as per Fig. 7 below and the resistance can be directly read over the LCD of the meter by pressing the test switch.



UNKNOWN RESISTANCE

Fig-7

PRECAUTIONS :

(1) Testing should start from higher ranges to lower ranges.

(2) It is necessary to reduce the resistance of the auxiliary earthing by moisting the soil near the electrodes or by using several earth electrodes in parallel.

(3) During tests, leads of predetermined resistances should be used and taken care of when taking reading particularly in the lower ranges i.e. the lead resistance should be measured before measurement of Earth Resistance or any other resistance.

RESULT:

The earth resistance using Megger tester is measured.

Experiment No : 7 Date :

CALCULATION OF ELECTRICAL ENERGYN FOR DOMESTIC PREMISES

Aim: To calculate the electrical energy for domestic loads.

Apparatus:

S.NO.	Name	Range	Type	Quantity
1	Dimmerstat or Variac	0-230V	1-Φ	1
2	Voltmeter	0-100V	MI	1
3	Ammeter	0-5A	MI	1
4	Wattmeter	300V, 5A	UPF	1
5	Energy meter	Induction	200 Rev/KWh	1
6	Bulb	180W		1
7	Stop watch	Digital		1
8	Connecting wires			Required

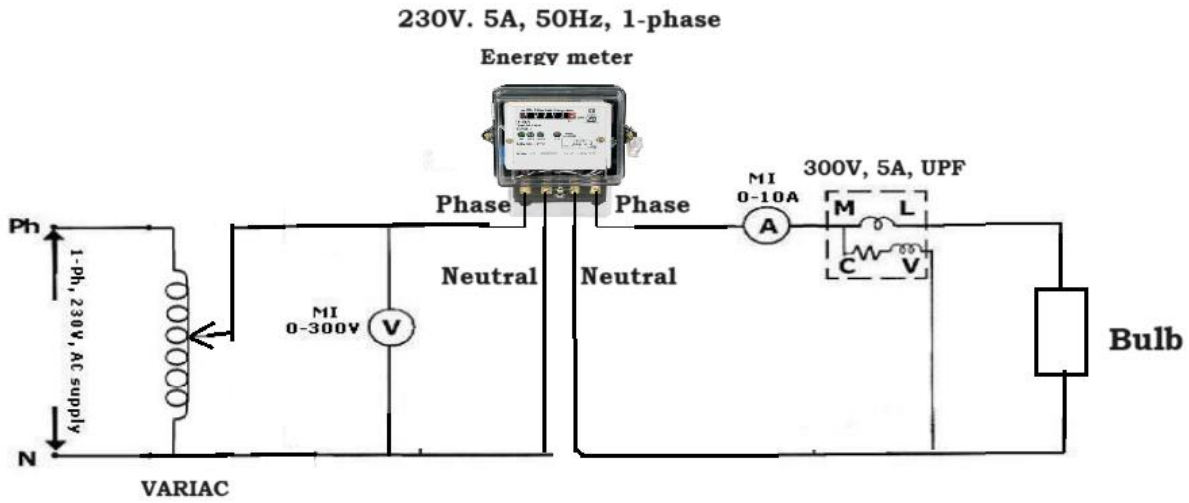
Theory:

An instrument that is used to measure either quantity of electricity or energy, over a period of time is known as energy meter or watt-hour meter. In other words, energy is the total power delivered or consumed over an interval of time t may be expressed as:

$$W = \int_0^t v(t)i(t)dt$$

If v(t) is expressed in volts, i(t) in amperes and t in seconds, the unit of energy is joule or watt second. The commercial unit of electrical energy is kilowatt hour (KWh). For measurement of energy in A.C. circuit, the meter used is based on “electro-magnetic induction” principle. They are known as induction type instruments. The measurement of energy is based on the induction principle is particularly suitable for industrial or domestic meters on the account of lightness and robustness of the rotating element. Moreover, because of smallness of the variations of voltage and frequency in supply voltage, the accuracy of the induction meter is unaffected by such variations. If the waveform of the supply is badly distorted, the accuracy, however, is affected. Basically, the induction energy meter may be derived from the induction watt-meter by substituting for the spring control and pointer an eddy current brake and a counting train, respectively. For the meter to read correctly, the speed of the moving system must be proportional to the power in the circuit in which the meter is connected.

Circuit Diagram:



PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Keep the single phase variac at zero volt position.
3. Now switch on the power supply.
4. Gradually vary the variac to apply the rated voltage (230 volts).
5. For different values of load, note down the readings of the ammeter, voltmeter, wattmeter and time taken for 05 revolutions of the disc.
6. Gradually vary the variac to minimum or zero volt position.
7. Switch off the power supply.
8. Calculate observed reading, actual reading, %error.

TABULAR COLUMN:

S.N.O.	Voltmeter (V)	Ammeter (A)	Wattmeter (W)	Time(t) for '5' Rev (sec)	Theoretical Energy (E1)	Practical Energy (E2)	%Error= (E1-2)/E2*100

Theoretical reading = E1
Practical reading = E2
MODEL CALCULATIONS:
Theoretical reading = No. of revolutions / (energy meter constant (k)
Where, no. of revolutions = 05
Energy meter constant k=1200 rev/kwh
Practical reading = W *t
%Error = [(E1-E2)/E2] *100

Precautions:

1) Measure the readings without parallax error.
2) Calculate the error at different loads.

Result:

The energy and %error for different loads are calculated.

VIVA QUESTIONS:

1. What is the working principle of energy meter?
2. What type of controlling torque is used in energy meter?
3. What is the purpose of using shading band in energy meter? .
4. How does energy meter differ from a watt meter?
5. What is the purpose of brake magnet in energy meter?
6. How braking torque can be adjusted in energy meters?
7. Which type of meter is energy meter?
8. What is creeping? How to avoid error due to creeping?
9. Why aluminium disc is preferred over copper disc?
10. Why induction type energy meter is preferred?

PART B: ELECTRONICS ENGINEERING LAB

Course Objectives:

• To impart knowledge on the principles of digital electronics and fundamentals of electron devices & its applications.

Course Outcomes: At the end of the course, the student will be able to

CO1: Identify & testing of various electronic components.
CO2: Understand the usage of electronic measuring instruments.
CO3: Plot and discuss the characteristics of various electron devices.
CO4: Explain the operation of a digital circuit.

List of Experiments:

1. Plot V-I characteristics of PN Junction diode A) Forward bias B) Reverse bias.
2. Plot V – I characteristics of Zener Diode and its application as voltage Regulator.
3. Implementation of half wave and full wave rectifiers
4. Plot Input & Output characteristics of BJT in CE and CB configurations
5. Frequency response of CE amplifier.
6. Simulation of RC coupled amplifier with the design supplied
7. Verification of Truth Table of AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates using ICs.
8. Verification of Truth Tables of S-R, J-K& D flip flops using respective ICs.

P-N JUNCTION DIODE CHARACTERISTICS	EXPT. NO: 1
	DATE:

Aim: Plot V-I characteristics of PN Junction diode A) Forward bias B) Reverse bias.

Apparatus: 0-30V Power Supply

0-1V Voltmeter

0-50mA Ammeter

0-500μA Ammeter

0-30V Voltmeter

1N4007 diode

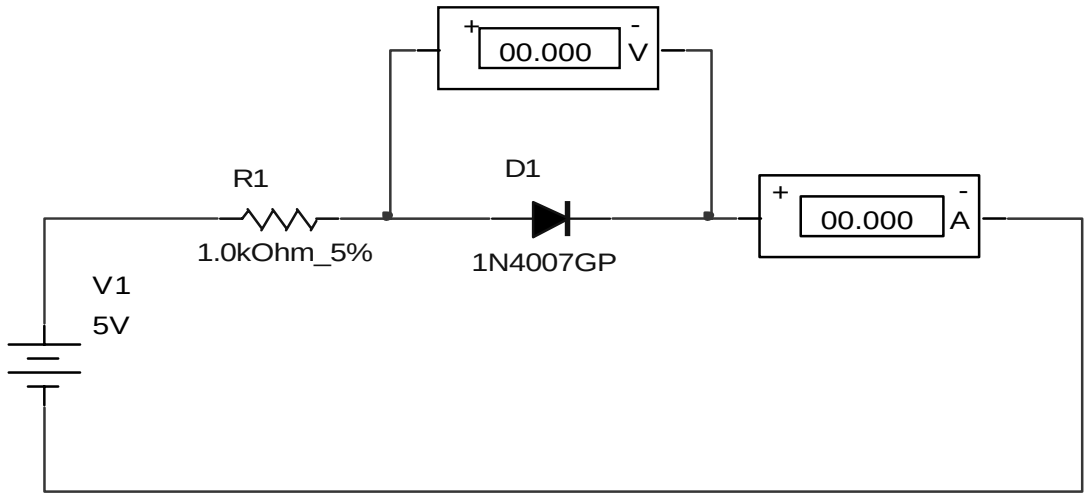
Theory:

Forward Bias: If P-type semiconductor is connected to the positive terminal of the battery and N-type Semiconductor is connected to negative terminal of the battery, this way of biasing is called as forward bias. In this biasing current is exponentially increasing with respective to applied voltage.

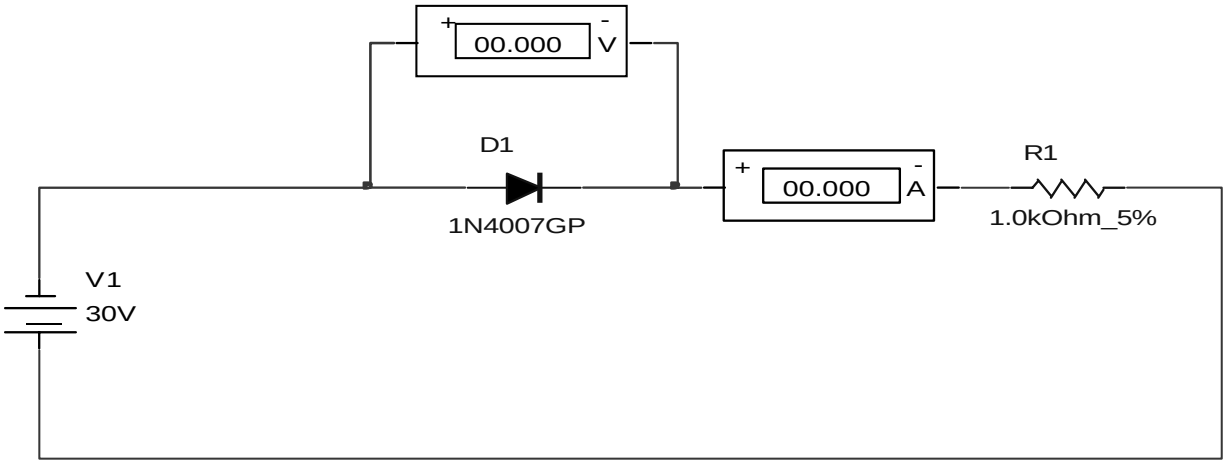
Reverse bias: If P-type semiconductor connected to negative terminal of the battery and N-type semiconductor is connected to the positive terminal of the battery is known as reverse bias. In reverse bias the current through the diode is I = -Io whose value is independent on applied voltages and which depends on minority carrier concentration and temperature. For every 10 degrees raise in temperature reverse saturation current becomes double.

Thus in forward bias diode offers less resistance and in reverse bias diode offers high resistance. Hence it is known as rectifier.

Circuit Diagram:



Forward Bias



Reverse Bias

Procedure:

1. Construct the Circuit as shown in Figure .Use 1N4007 and forward bias it. Get the circuit verified.
2. Adjust the voltage in suitable increments until the current through the diode (Ammeter reading) is maximum allowable value. Note the voltage across the diode.
3. Decrease the voltage applied to the diode in steps and note the ammeter and voltmeter reading. Sample readings are shown below.
4. To reverse bias the diode construct the circuit as shown in figure . use 1N4007 diode.
5. Adjust the Power supply gradually up to 20V observing the micro ammeter reading.
6. Decreasing the voltage in convenient steps and note the ammeter and voltmeter reading.

Observations:

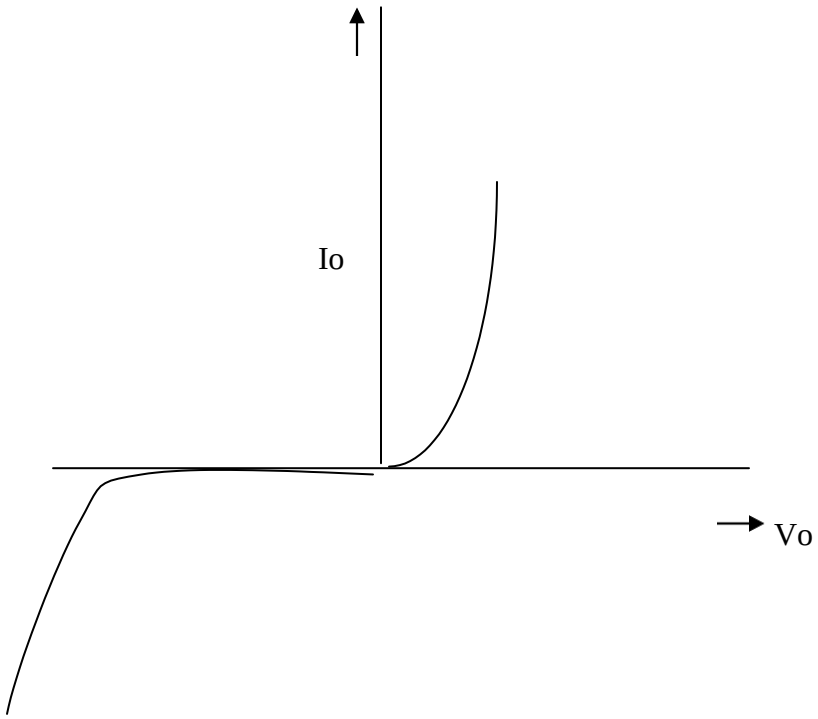
Forward Bias:

Voltmeter Reading (V)										
Ammeter Reading (mA)										

Reverse Bias:

Voltmeter										
Reading (V)										
Ammeter Reading (μA)										

Graphs: Draw graphs showing volt ampere relation for 1N4007 diode. Sample Graph is as shown in figure.



Results: 1. Static forward resistance =

2. Static reverse resistance =
3. Dynamic forward resistance =
4. Dynamic reverse resistance =

Viva Questions :

1. What is meant by P- type layer?
2. What is meant by N- type layer?
3. What is the function of p-n junction diode?
4. What is meant by forward bias of p-n junction diode?
5. What is meant by reverse bias of p-n junction diode?
6. Define cut-in voltage of p-n junction diode.
7. What is meant by depletion layer in p-n junction diode?

ZENER DIODE CHARACTERISTICS	EXPT. NO: 2
	DATE:

Aim: Plot V – I characteristics of Zener Diode and its application as voltage Regulator.

Apparatus: 0-30V Power Supply

0-1V Voltmeter

0-50mA Ammeter

0-500μA Ammeter

0-30V Voltmeter

Zener diode BZX 4.2V or BZX 5.1V or 1Z 6.2V

Theory: In forward bias it acts as similar to the diode. In the reverse bias it acts as regulator because its doping concentration is higher than the ordinary diode, due to this a large electric field intensity is developed at the known as Zener Break. The diode which adopts this is zener diode.

VOLTAGE REGULATOR

The zener diode should maintain a constant output voltage against variations in input voltage Vin, or load resistance R_L.

Basically there are two type of regulations such as:

Line Regulation: In this type of regulation, series resistance and load resistance are fixed, only input voltage is changing. Output voltage remains the same as long as the input voltage is maintained above a minimum value.

Line regulation can be defined as the percentage change in the output voltage for a given change in the input voltage.

$$Line\ regulation = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}} \right) \times 100\%$$

Load Regulation: In this type of regulation, input voltage is fixed and the load resistance is varying. Output volt remains same, as long as the load resistance is maintained above a minimum value.

Load regulation can be defined as the percentage change in the output voltage from no-load (NL) to full-load (FL).

$$Load\ regulation = \left(\frac{V_{NL} - V_{FL}}{V_{FL}} \right) \times 100\%$$

Where:

V_{NL} = the no-load output voltage

V_{FL} = the full-load output voltage

Circuit diagram:

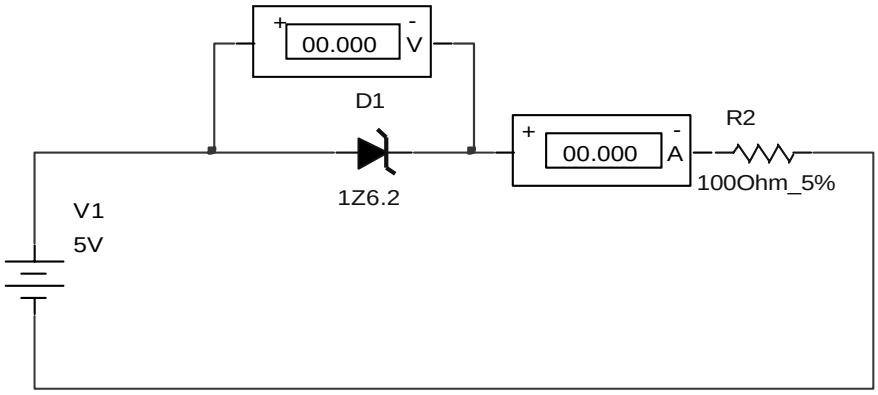


Fig.1.Zener diode Forward bias

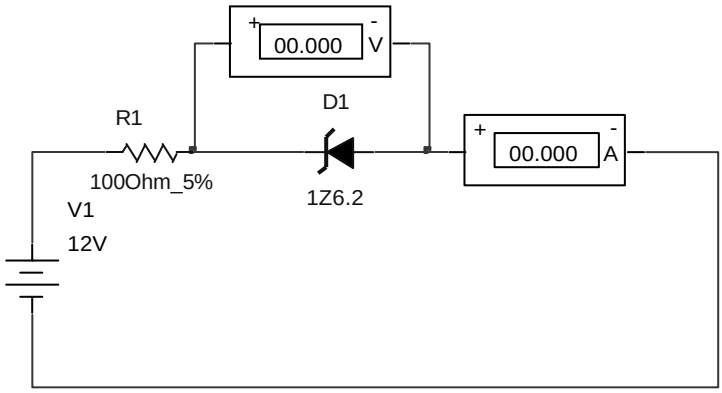


Fig.2.Zener diode Reverse bias

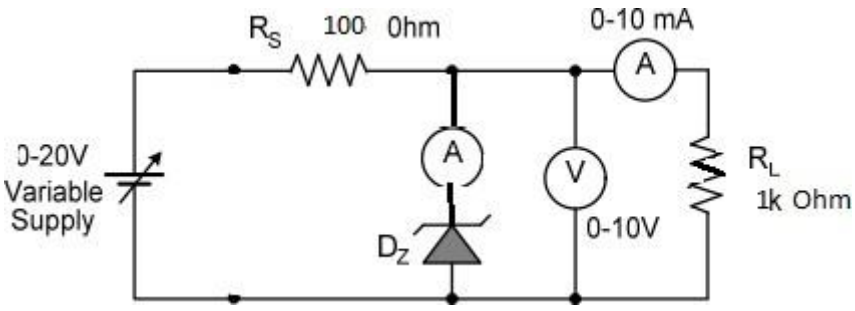


Fig.3.Zener Voltage Regulator with a Variable Input Voltage

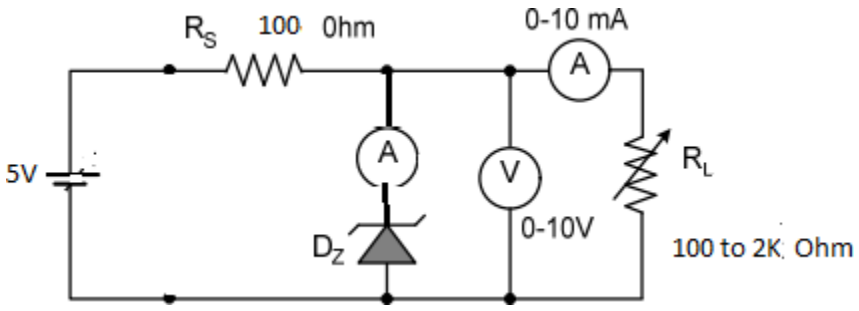


Fig.4.Zener Voltage Regulator with a Variable Load Resistance

A.PROCEDURE FOR FORWARD BIAD AND REVERSE BIAS:

1. Construct the Circuit as shown in Figure .Use 1Z 6.2V and forward bias it. Get the circuit verified.
2. Adjust the voltage in suitable increments until the current through the diode (Ammeter reading) is maximum allowable value. Note the voltage across the zener diode.
3. Decrease the voltage applied to the zener diode in steps and note the ammeter and voltmeter reading. Sample readings are shown below.
4. Construct the circuit as shown in figure using 1Z 6.2V zener diode to reverse bias the diode.
5. Adjust the power supply gradually until we get 70mA.Note the voltage across the diode.
6. Decrease the voltage applied in convenient steps and each step, note voltage across the diode and ammeter reading.

Observations:

Forward Bias:

Voltmeter Reading (V)										
Ammeter Reading (mA)										

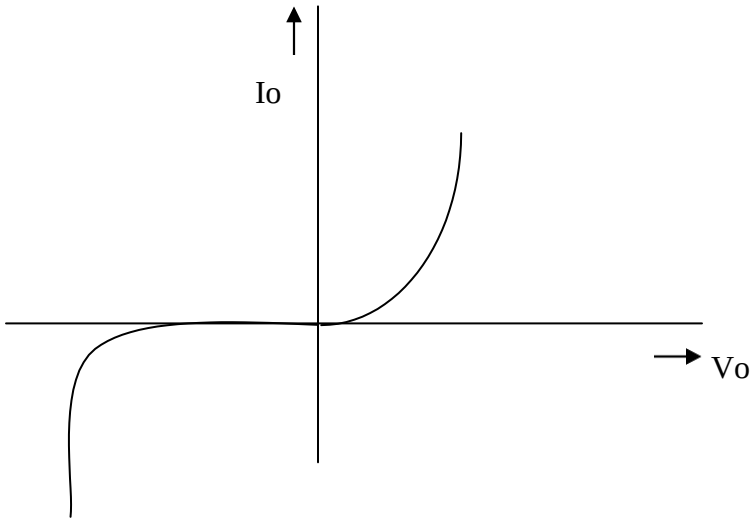
TABLE1:FORWARD BIAS CHARACTERISTICS

Reverse Bias:

Voltmeter Reading (V)										
Ammeter Reading (mA)										

TABLE2:REVERSE BIAS CHARACTERISTICS

Graphs: Draw graphs showing volt ampere relation for 1Z 6.2V zener diode. Sample Graph is as shown in figure.



Results: 1. Cut in Voltage =

2. Break down Voltage =

B.PROCEDURE FOR LINE REGULATION:

1. Connect the circuit as shown in fig.
2. Vary DC voltage 0 to 20V step by step.
3. Note the Load current(I_L), zener current(I_z), Output voltage(V_o)
4. Calculate the voltage regulation.
5. Draw the graph between output voltage(y-axis) and input voltage (x-axis).

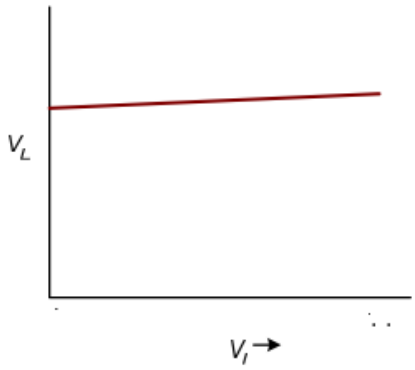
Serial No.	Unregulated supply voltage(V_S) V	Load Current(I_L) mAmp	Zener Current(I_Z) mAmp	Regulated Output Voltage(V_O) V	% Voltage Regulation

TABLE 3.LINE REGULATION

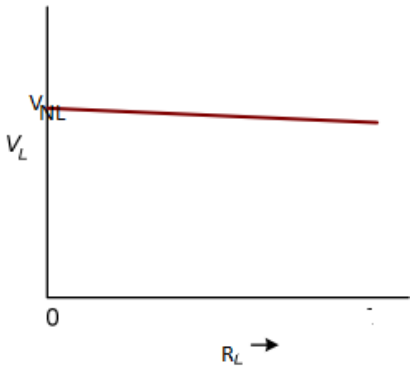
C.PROCEDURE FOR LOAD REGULATION:

1. Connect the circuit as shown in fig.
2. Keeping input voltage is fixed and Noted down output voltage as V_{NL}
3. Vary the Load Resistance (R_L) step by step.
4. Note the Load current(I_L), zener current(I_z), Output voltage(V_o)
5. Calculate the voltage regulation.
6. Draw the graph between output voltage(y-axis) and Load Resistance (x-axis).

EXPECTED OUTPUT PLOTS



Line Regulation



Load Regulation

Viva Questions :

1.What is meant by Avalanche effect?

2.What is meant by Zener effect?

3.What is meant by static and dynamic resistance of zener diode?

4.What is meant by Zener break down voltage?

5.What is Voltage regulator, Line Regulation and Load Regulation?

HALF WAVE RECTIFIER

EXPT. NO :3 (a)

DATE:

Aim : 1.To Examine the input and output waveforms of a Half wave rectifier.

2.To find the ripple factor,

3.To find the regulation

4.To repeat the objectives 1,2&3 with Capacitor filter.

Apparatus: 230V/0-9V Transformer

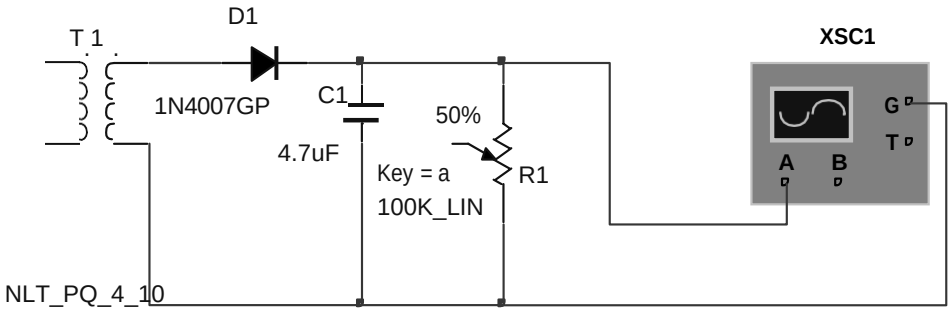
Diode1N4007, Capacitor 470μF, DRB, Multi Meter, CRO.

Theory : As per the circuit diagram, it contains transformer and one diode, DRB, Capacitor. During the positive swing of power supply, the diode acts as forward bias condition. Hence it offers very less resistance. Thus whatever the input signal is applied transmitted to the load resistance when the negative swing of the A.C signal is applied to the diode, it acts as reverse bias connection Since it offers as high resistance. In this no signal is allowed to the load. Thus it gives Half wave output signal .The amount of A.C signal is present in output wave form is measured by ripple factor.

$$\text{Ripple factor} = \frac{V_{rms}}{V_{dc}}$$

$$\text{Percentage of Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

Circuit diagram:



Half wave rectifier

Procedure : 1.Connect the circuit as shown in figure.

2. Use the diode 1N4007 and load resistance R_L . Do not connect Capacitor.
3. Observe the Voltage across the secondary of the transformer and across the output terminals using CRO.
4. Vary the load resistance in convenient steps and note the A.C voltage and D.C voltage across the load.
5. Connect the Capacitor across the load and repeat the procedure 1,2&3

Observations : (without filter Capacitor)

V_{AC} No load = V_{DC} No load =

S.No	Load (R_L)	V_{AC}	V_{DC}	Ripple Factor	% Reg.

(with filter Capacitor)

V_{AC} No load = V_{DC} No load =

S.No	Load (R_L)	V_{AC}	V_{DC}	Ripple Factor	% Reg.

Results: Average Ripple factor without filter :

Average Ripple factor with filter :

Average % Regulation without filter :

Average % Regulation with filter :

Viva Questions:

1. What is the function of half wave rectifier (HWR)?
2. What is meant by voltage regulation of HWR?
3. What are the applications of HWR?
4. What is the value of peak inverse voltage of HWR?
5. What is the value of ripple factor in HWR?

BRIDGE RECTIFIER

EXPT. NO: 3 (b)

DATE:

Aim : To Rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Bridge

rectifier with and without Capacitor filter.

Apparatus:

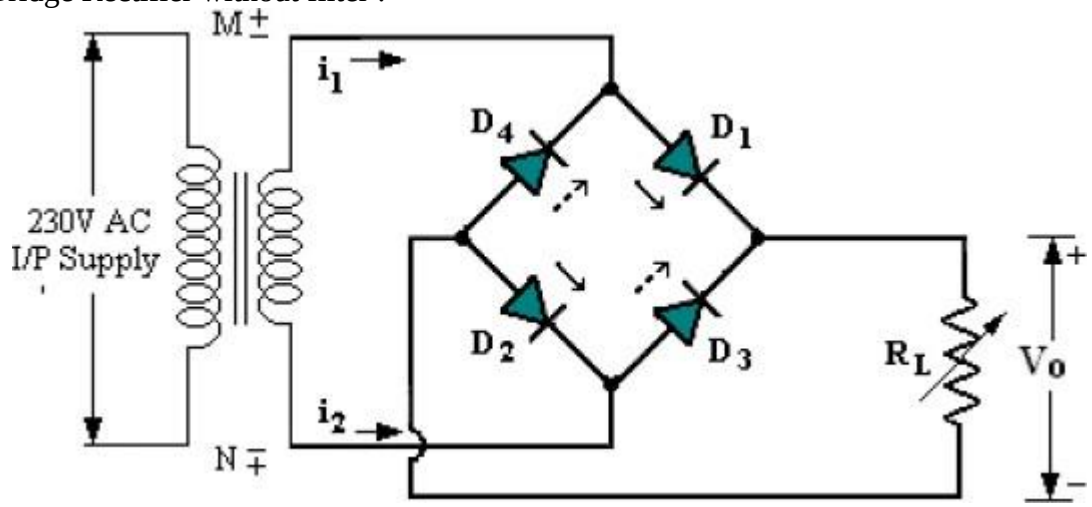
S.NO	Name	Range/Value	Quantity
1	Transformer	230V / 12V	1
2	Diode	1N4007	4
3	Multi meter	--	1
4	Resistor	1 kΩ, 2.2 kΩ,3.3 kΩ & 10 kΩ	1 Each
5	Capacitor	4.7μF	1
6	Bread Board and Connecting wires	--	1 set
7	Dual Trace CRO	20 MHz	1

Theory:

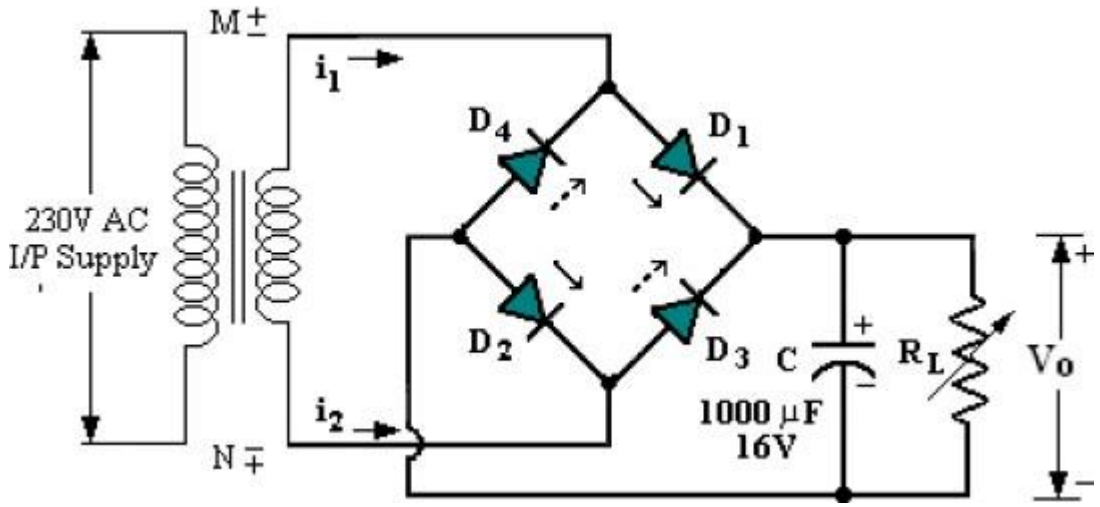
Full Wave Bridge Rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown in figure. The four diodes labeled D_1 to D_4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load, During the negative half cycle of the supply, diodes D3 and D4 conduct in series, but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

Circuit Diagram:

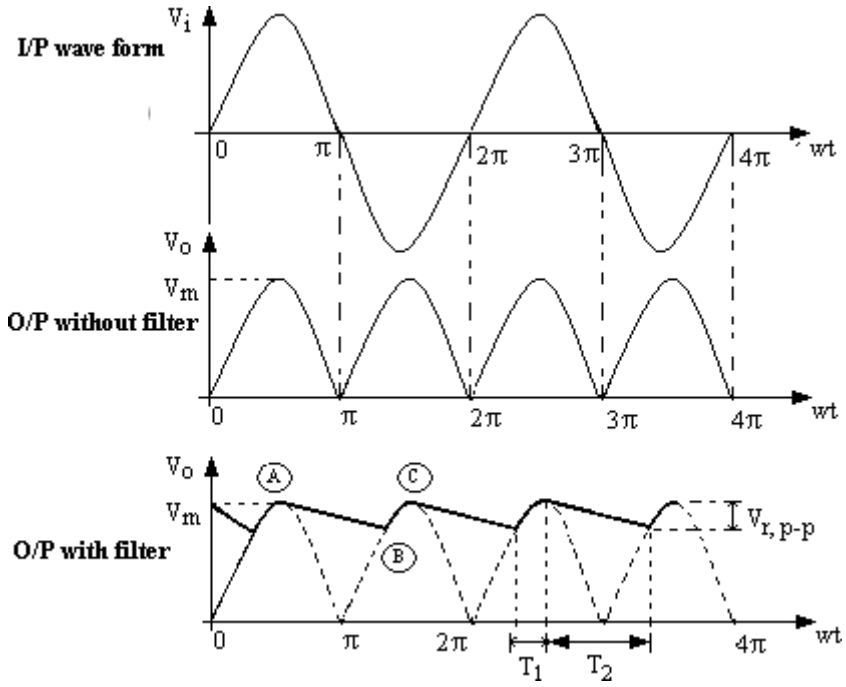
Bridge Rectifier without filter :



Bridge Rectifier with filter :



Waveforms :



Procedure :

WITHOUT FILTER:

1. Connect the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the resistance RL of value 1kΩ
4. Connect the Multimeter at output terminals and vary the load resistance from 1kΩ to 10KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance and note down no load voltage Vdc (V no load)
6. observe and note down the Input and Output Wave form on Graph Sheet.
7. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of Regulation, $\%\eta = \frac{V_{dc\ no\ load} - V_{dc\ full\ load}}{V_{dc\ full\ load}} * 100$

WITH CAPACITOR FILTER:

1. Connect the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

Observations :

(without filter Capacitor)

V_{AC} No load = V_{DC} No load =

S.No	Load (R_L)	V_{AC}	V_{DC}	Ripple Factor	% Reg.

(with filter Capacitor)

V_{AC} No load = V_{DC} No load =

S.No	Load (R_L)	V_{AC}	V_{DC}	Ripple Factor	% Reg.

Results: Observed Input and Output Wave forms and Calculated ripple factor and percentage of regulation in Full-wave Bridge rectifier with and without filter.

Viva Questions:

1. What is the function of full-wave rectifier (FWR)?
2. What is meant by voltage regulation of FWR?
3. What are the applications of FWR?
4. What is the value of peak inverse voltage of FWR?
5. What is the value of ripple factor in FWR?

TRANSISTOR CHARACTERISTICS: COMMON EMITTER (CE)	EXPT. NO: 4 (a)
	DATE :

AIM:- A. To plot the input and output characteristics of a transistor connected in common emitter configuration .

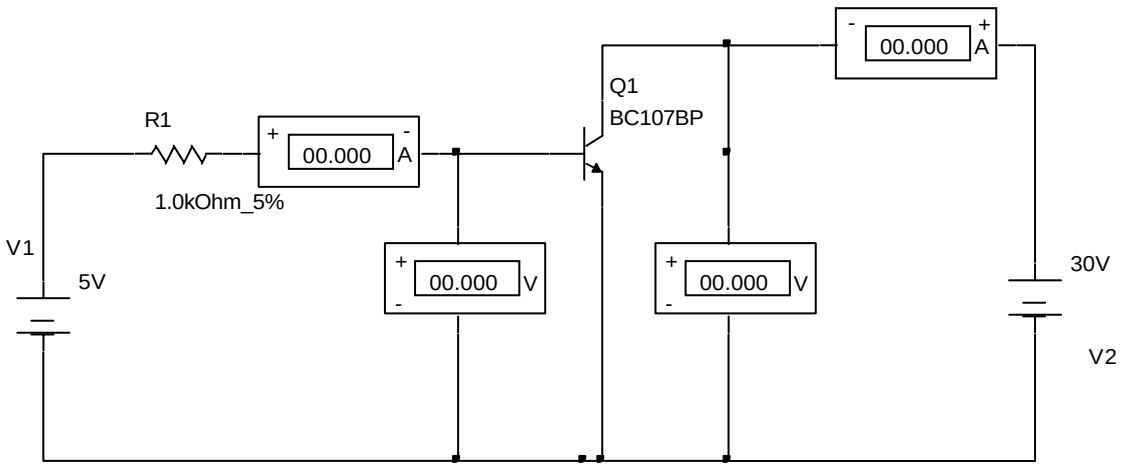
APPARATUS:-

1. (0-30 V) Power supply
2. (0-10Ma) ammeter
3. (0-1V) Volt Metter
4. (0-30V) Volt Metter
5. BC 107

PROCEDURE:-

1. Connect the circuit as shown in the figure.
2. Make V_{CE} = OPEN
3. Vary the 5V supply in convenient steps and note the values of I_B and V_{BE}.
4. Adjust 0-30V power supply so that V_{CE}=0V And fix it.
5. Vary the 5V supply in convenient steps and note the values of I_B and V_B and V_{BE}.
6. Steps repeat 4 and 5 for V_{CE} =2V.
7. Sample observations are given to obtain out put characteristics family.
8. Adjust 5V supply and fix the value of I_B =50μA.
9. Vary the 0-30V Power supply in convenient steps and note the value of I_C And V_{CE}.
10. Repeat steps 8 for I_B=100μA To 150μA.

CIRCUIT:-



TABULAR FORM:-

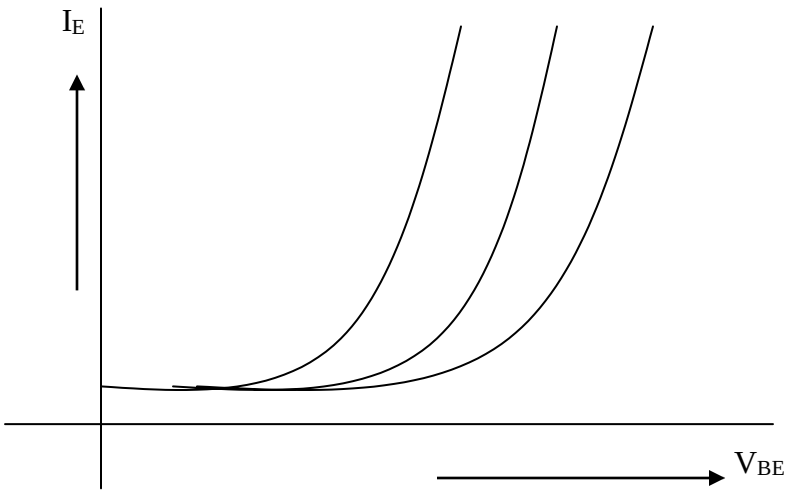
INPUT

V_{CE}=0V		V_{CE}=2V	
V_{BE}	I_BμA	V_{BE}	I_BμA

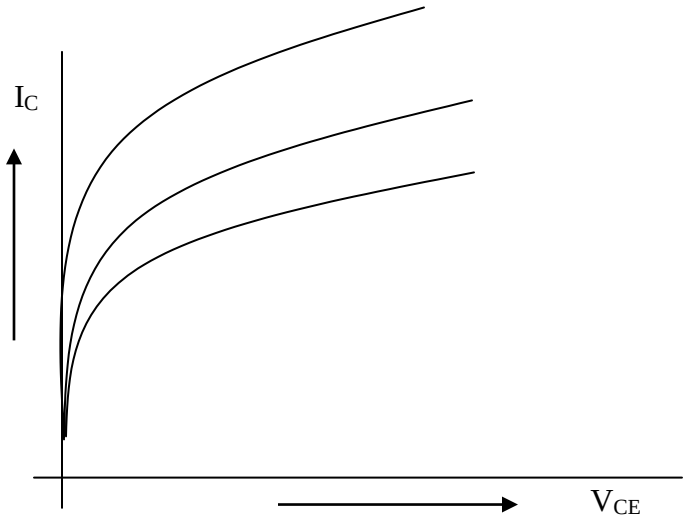
OUTPUT

I_B=50μA		I_B=70μA		I_B=100μA	
V_{CE}	I_C	V_{CE}	I_C	V_{CE}	I_C

GRAPH:- (INPUT)



GRAPH : (OUTPUT)



RESULT:- Characteristics of CE are studied.

Viva Questions:

1.Give the relation betwee I_B, I_C and I_E

2.Give the relation between I_{CEO} and $I_{CBO.}$

3.Define the transport factor.

4. Define saturation region, cut-off region and active region.

TRANSISTOR CHARACTERISTICS:COMMON BASE (CB)	EXPT.NO: 4(b)
	DATE :

Aim: B. To plot the input and output characteristics of a transistor connected in common Base configuration .

.

Apparatus : 1. Transistor BC 547/BC 107
2. Resistor 1KΩ
3. RPS
4. Voltmeter 0-10V, 0-30V
5. Ammeter 0-50mA, 0-100mA
6. Breadboard ,Connectors

Theory : In a common Base transistor base terminal is connected common to both the nput (Emitter – Base) voltage and the output (collector –base) voltage . Voltmeters and Ammeters are connected to measure the input and output voltages and currents.

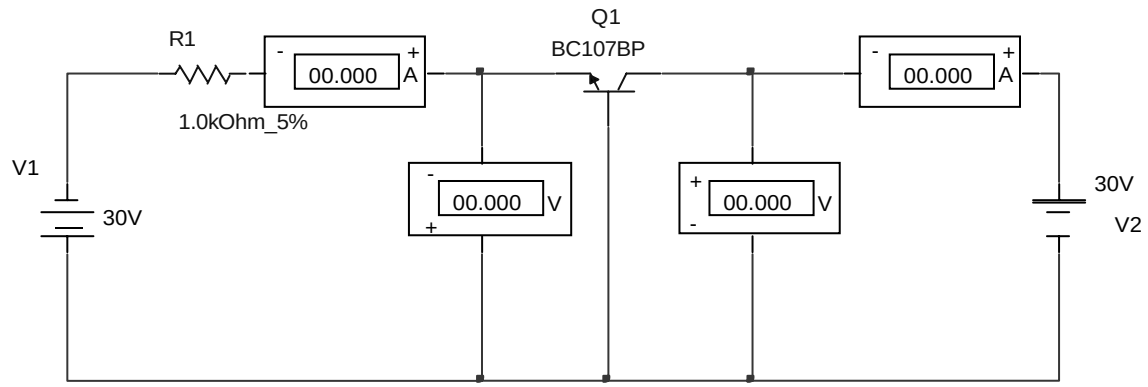
Input Characteristics:

To determine the input characteristics, the output (Collector-Base) Voltage is maintained constant ,and the input (Emitter-Base) voltage is set at several convenient levels. For each level of the input voltage, the input current (Emitter current) is recorded.

Output Characteristics:

To determine the output characteristics the input (Emitter) Current is held constant at each of several fixed levels. For each fixed level of I_E, the output voltage V_{CB} is adjusted in convenient steps, and the corresponding levels of collector current are recorded.

CIRCUIT DIAGRAM:-



PROCEDURE:-

1. Connections are given as per the circuit diagram.
2. I/P Characteristics:-

   (a) . Set the output voltage V_{CB} as constant and vary the input voltage V_{BE} in convenient steps and note down the input current I_E at each step.

   (b) . Repeat step 2 for different values of output voltage V_{CB}.

3. O/P Characteristics:-

   (a) . Set the input current IE as constant adjusting the input power supply.

   (b) . Vary the output voltage V_{CB} in convenient steps and note down the output current I_C at each step.

4. Repeat steps 4 & 5 for constant values of I_E.

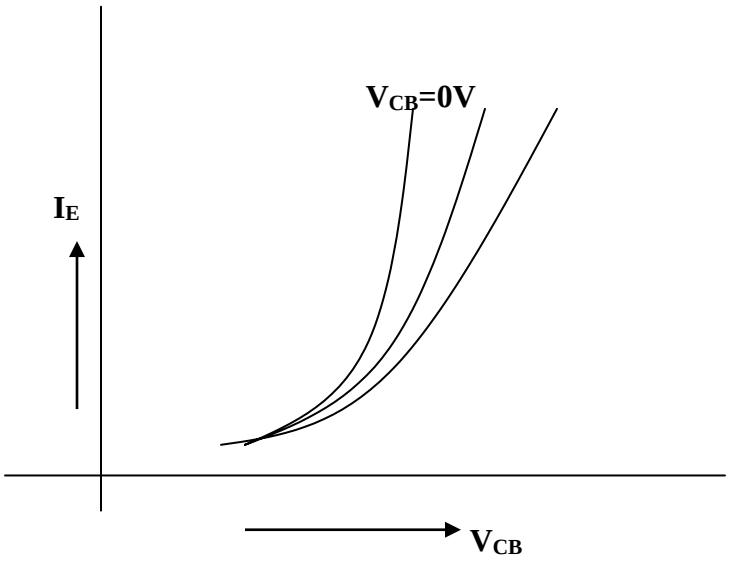
TABULAR READINGS:

V_{CB}= 0V		**V_{CB}= 1V**		**V_{CB}= 2V**	
V_{BE} (V)	**I_E (mA)**	**V_{BE} (V)**	**I_E (mA)**	**V_{BE} (V)**	**I_E (mA)**

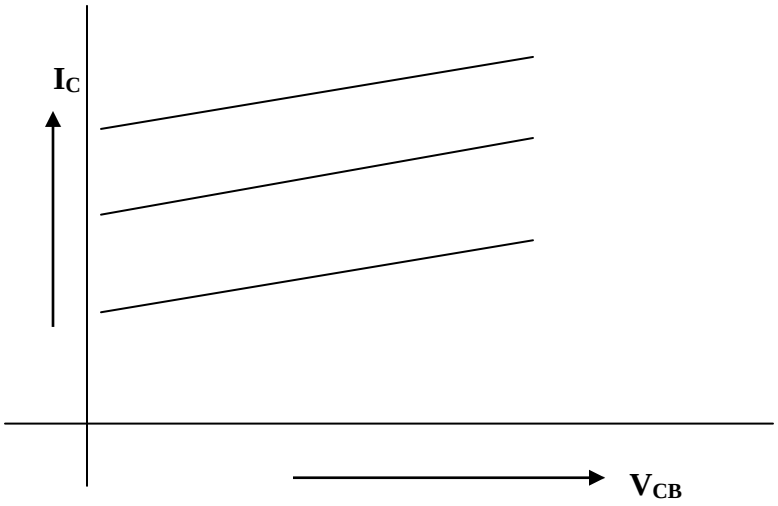
OUTPUT CHARACTERISTICS:

I_E =		**I_E =**		**I_E =**	
V_{CB} (V)	**I_C (mA)**	**V_{CB} (V)**	**I_C (mA)**	**V_{CB} (V)**	**I_C (mA)**

GRAPH:- (INPUT)



GRAPH: (OUTPUT)



RESULT:

Viva Questions:

1. Explain Early effect in CB configuration?
2. Give the relation betweenI_B and I_C .
3. Define large signal current gain.
4. Define emitter efficiency.

FREQUENCY RESPONSE OF CE AMPLIFIER	EXPT. NO: 5
	DATE:

AIM:- To study the frequency response characteristics of single RC COUPLED AMPLIFIER.

APPARATUS:-

1. Transistor (BC 107)
2. Resistors- 2.2 KΩ,220Ω,1KΩ
3. Capacitors- 10μF,100μF
4. Function generator
5. CRO

THEORY:-

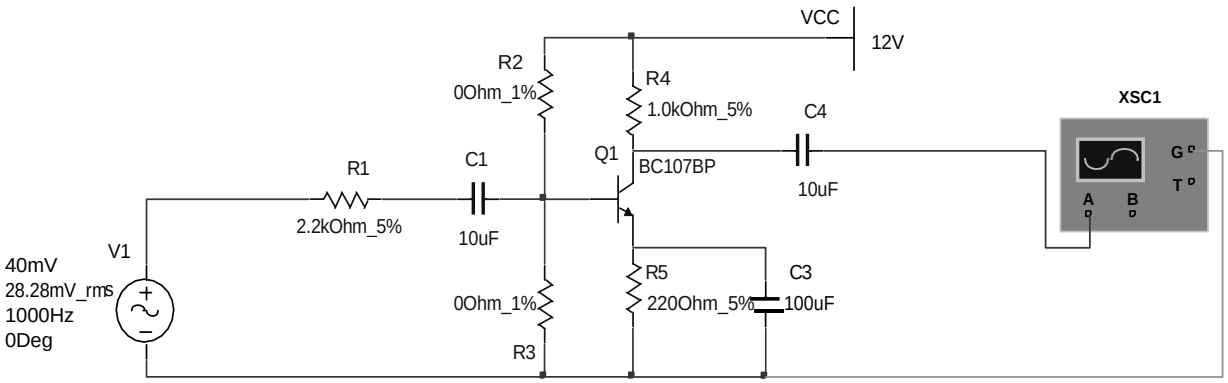
In the CE AMPLIFIER its current gain and voltage gain are high resulting in higher power gains compared with the other configurations. Its input impedance is medium high and output impedance is medium. In the circuit emitter resistance provides bias stabilization due to dc generative feedback. But this also reduces AC gain since same feedback is there for AC Also. AC degenerative feed back is eliminated by bypassing RC using a large capacitor. This bypass capacitor affects the frequency response of the amplifier.

Frequency response is the curve drawn on a semi log paper between gain (usually in db) of the amplifier and the input signal frequency. Generally frequency is taken along X-axis on a log scale and gain (db) along Y-axis on a liner scale. The amplifier maintains constant gain in the mid band of frequencies. The gain below the lower cut off frequency is rolling down. This is because, during the low frequencies the resistance of the input capacitor C_B very high. So amplification is poor. During the high frequencies, input capacitor acts as short circuit. But the reactance of emitter bypass capacitor C_E is low.

FORMULAE:-

BAND WIDTH: (F_h-F_L)KHZ Where F_h= Upper cut off frequency. F_L= Loewr cut off frequency.

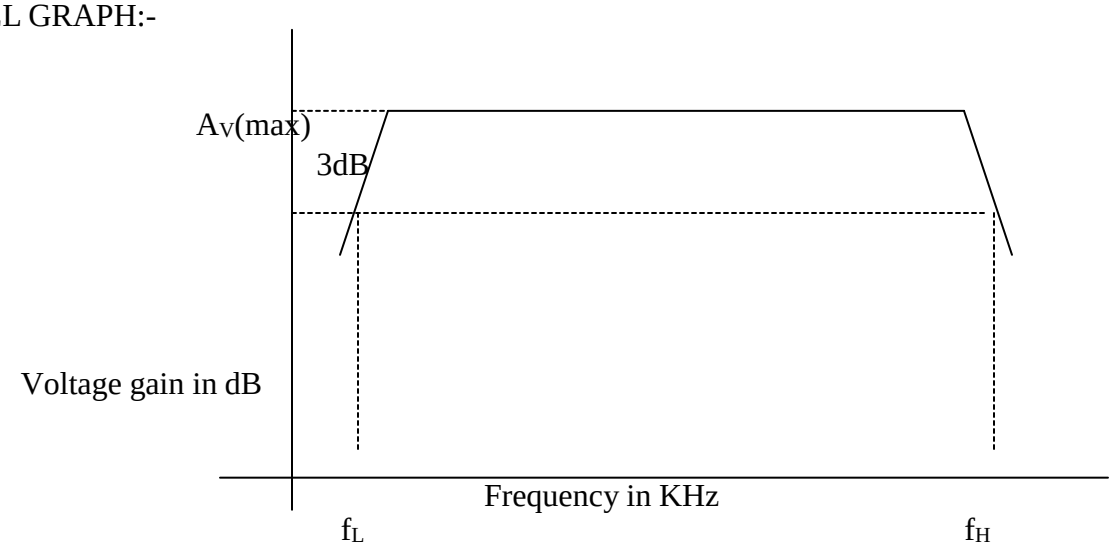
CIRCUIT DIAGRAM:-



PROCEDURE:-

1. Connect the power cord of the unit to AC mains and connect the output of the signal generator to the input of CE amplifier.
2. Feed a sine wave of amplitude about 40 mv , changing the frequency of signal generator, measure the voltage output using a FET Voltmeter and simultaneously observe the waveform on oscilloscope.
3. Tabulate the results and plot the curve frequency (f) versus voltage gain (Av) in db.
4. Compute the 3-db bandwidth of the CE amplifier from the graph.
5. Connect the variable resistance RL to the output and adjust its value so that output voltage falls to half of its value when not connected. This gives the output impedance of the CE Amplifier.

MODEL GRAPH:-



TABULAR READINGS:-

S . No	Frequency in HEz	Output Voltage (Vo) in Volts	Gain = (Vo/VIn)	Gain in db = 20log(Vo/Vin)
	10 20 20 .. 100 200 .. 1000 2000 .. 1000KHz 2000KHz 3000KHz			

RESULT:-

Thus the experiment on CE amplifier has been done and the bandwidth been found to be .....kHz.

Viva Questions:

1. Compare CE and CB amplifiers.
2. What are the Applications of CE amplifier?
3. Compare CE and CC amplifiers.

SIMULATION OF RC COUPLE AMPLIFIER	EXPT. NO: 6
	DATE:

AIM:- To design and draw the frequency response of RC COUPLED AMPLIFIER using MULTISIM.

APPARATUS:-

1. Transistor (BC 107)
2. Resistors- 2.2 KΩ,220Ω,1KΩ
3. Capacitors- 10μF,100μF
4. Function generator
5. CRO

THEORY:-

RC Coupled amplifier consists the following elements:

(i) Biasing circuit: The resistances R1, R2 and RE form the biasing and stabilization circuit.

(ii) Input capacitance Cin: This is used to couple the signal to the base of the transistor. If this is not used, the signal source resistance will come across R2 and thus change the bias. The capacitor Cin allows only a.c. signal to flow.

(iii) Emitter bypass capacitor CE : This is connected in parallel with RE to provide a low reactance path to the amplified a.c. signal. If it is not used, then amplified a.c. signal flowing through RE will cause a voltage drop across it, thereby shifting the output voltage.

(iv) Coupling capacitor C : This is used to couple the amplified signal to the output device. This capacitor C allows only a.c. signal to flow.

When a weak input a.c. signal is applied to the base of the transistor, a small base current flows. Due to transistor action, a much larger a.c. current flows through collector load RC, a large voltage appears across RC and hence at the output. Therefore, a weak signal applied to the base appears in amplified form in the collector circuit. Voltage gain (Av) of the amplifier is the ratio of the amplified output voltage to the input voltage. The frequency response curve obtained will be of the form as shown in Fig. It can be seen that the gain decreases at very low and very high frequencies, but it remains constant over a wide range of mid-frequency region and Band Width to be calculated.

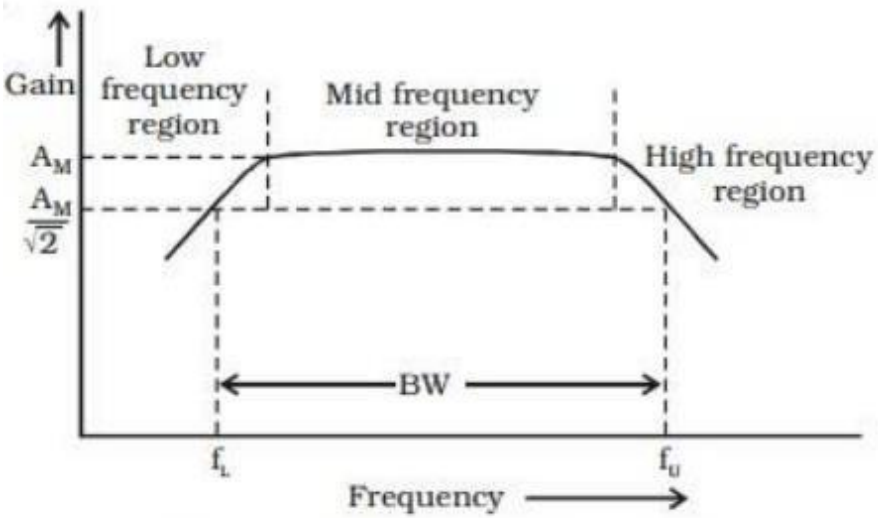


Fig Frequency response curve

DESIGN

Let **Vcc=20V** Ic=10mA ;V_{CE}=Vcc/2=10V ;Pd=$V_{CEQ}I_{CEQ}$=10*10*1e-3=100mw

$V_E \approx Vcc/10=20/10=2V$;$I_E \approx Ic$;$R_E=V_E/I_E=2/10*1e-3=200\Omega$

select standard value RE=220Ω

V_E=2*10*1e-3=2.2V

Rc=(Vcc-V_{CE}-V_E)/Ic =(20-10-2)/10*1e-3=780Ω

select standard value Rc=820Ω

$R2 \leq \beta R_E/10$ $\beta=G_{FE}$=125(min)

$\leq$2750Ω

select R2=2.7KΩ

V_B=0.7+2.2=2.9V

2.9=(2.7*1e3*20)/(R1+2.7*1e3)

= 15920

select standard value of 18KΩ =R1

Lower cut off frequency f1=100Hz

C2≈0.22µF

C1=C2=0.22µF

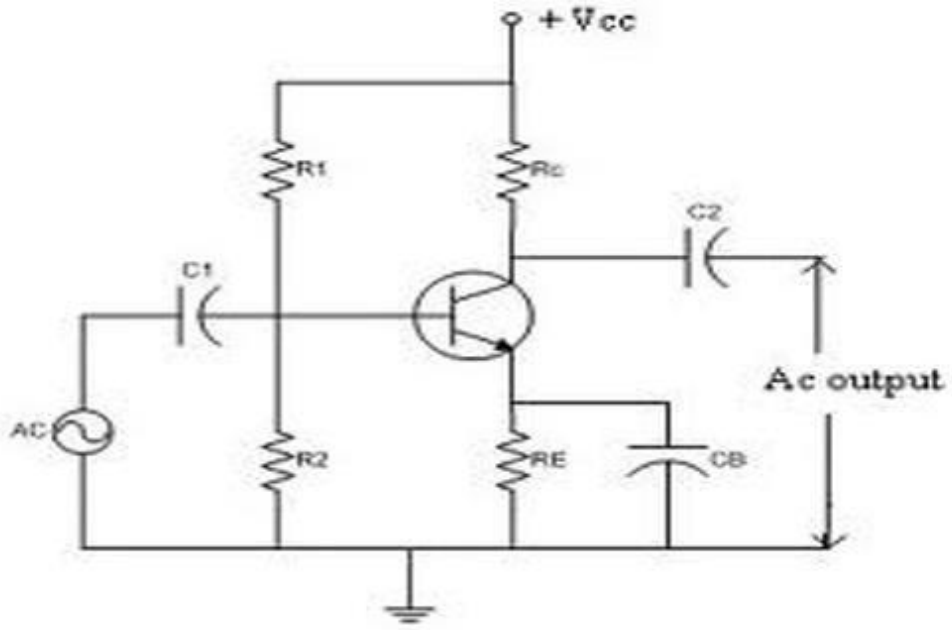
C_E=1/(2JIf1Xc2) Xc2=hie/(1+hfe) hie=1.5K, hfe=60

=24.6Ω

C_E=64.69µF

Select standard value of 47µF or 100µF

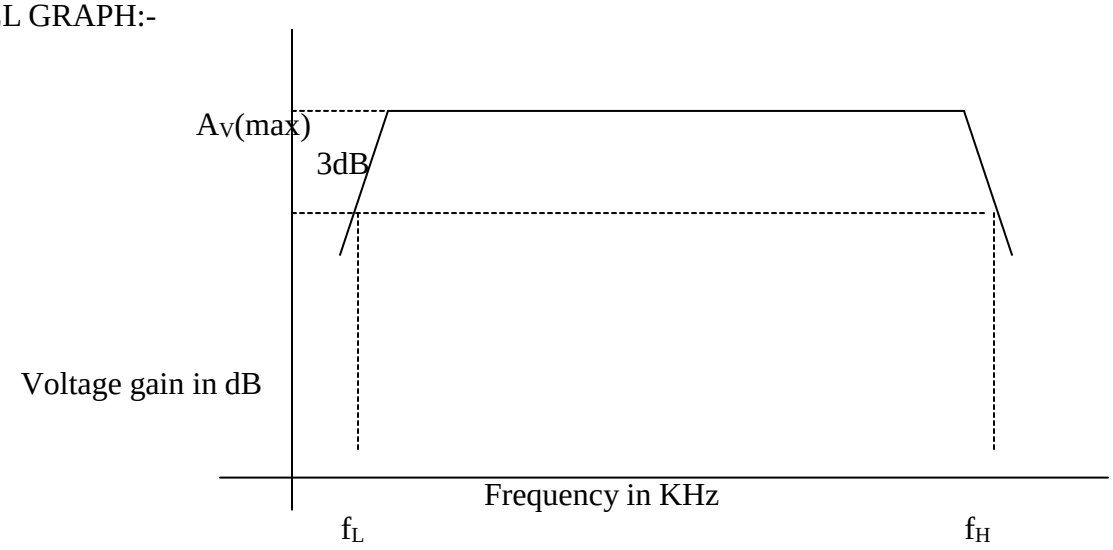
CIRCUIT DIAGRAM:-



PROCEDURE:-

1. Open MULTISIM tool and select proper component as per above the design the procedure and connect the circuit as shown in fig.
2. Apply a sinewave amplitude about 50mV measure the voltage output using a FET Voltmeter and simultaneously observe the waveform on oscilloscope.
3. Increase the frequency step by step and tabulate .
4. Tabulate the results and plot the curve frequency (f) versus voltage gain (Av) in db.
5. Compute the 3-db bandwidth of the CE amplifier from the graph.
6. Connect the variable resistance RL to the output and adjust its value so that output voltage falls to half of its value when not connected. This gives the output impedance of the CE Amplifier.

MODEL GRAPH:-



TABULAR READINGS:-

S . No	Frequency in Hz	Output Voltage (Vo) in Volts	Gain = (Vo/VIn)	Gain in db = 20log(Vo/Vin)
	10 20 20 .. 100 200 .. 1000 2000 .. 1000KHz 2000KHz 3000KHz			

RESULT:-

Thus the experiment on CE amplifier has been done and the bandwidth been found to be .....kHz.

Viva Questions:

1. Compare CE and CB amplifiers.
2. Compare CE and CC amplifiers.
3. Which is best amplifier?
4. What is Band width of Amplifier?
5. What are the Applications of CE amplifier?

STUDY OF LOGIC GATES	EXPT. NO: 7
	Date:

a) AIM:

To study of logic gates and verify their truth tables using IC's.

APPARATUS REQUIRED:

i) IC 7408, IC 7432, IC 7404

ii) LEDs

iii) Breadboard

iv) Connecting Wires

THEORY:

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output. OR, AND, NOT are basic gates.

i) AND GATE: (IC 7408)

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

ii) OR GATE: (IC 7432)

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

iii) NOT GATE: (IC 7404**)**

The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high.

iv) NAND GATE: (IC 7400)

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

v) NOR GATE: (IC 7402**)**

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

vi) Ex-OR GATE: (IC 7486)

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

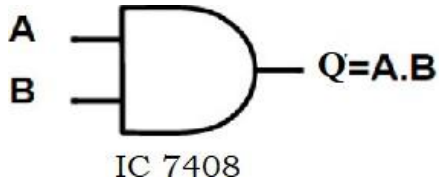
vii) Ex-NOR GATE: (IC 74266)

The output is low when any one of the inputs is high. The output is high when both the inputs are low and both the inputs are high.

SYMBOL ,PIN DIAGRAMS & TRUTH TABLE:

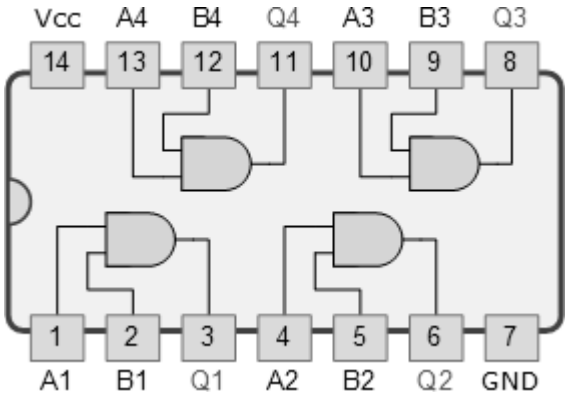
i) AND GATE:

SYMBOL:



IC 7408

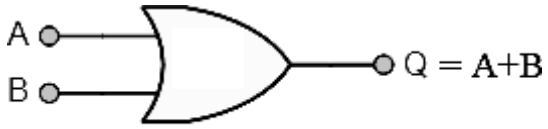
PIN DIAGRAM:



TRUTH TABLE:

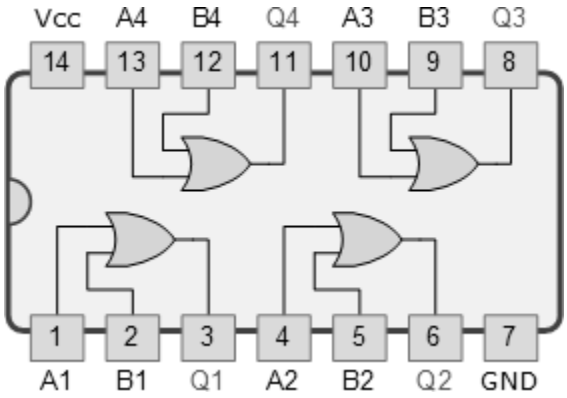
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

ii) OR GATE:
SYMBOL:



IC 7432

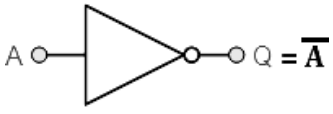
PIN DIAGRAM:



TRUTH TABLE:

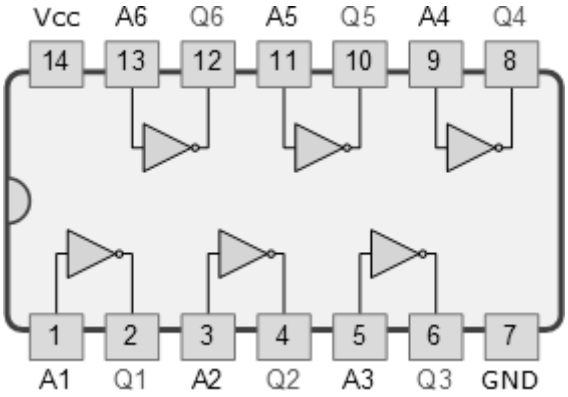
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

iii) NOT GATE:
SYMBOL:



IC 7404

PIN DIAGRAM:

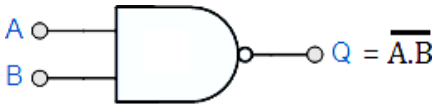


TRUTH TABLE:

A	$\overline{A}$
0	1
1	0

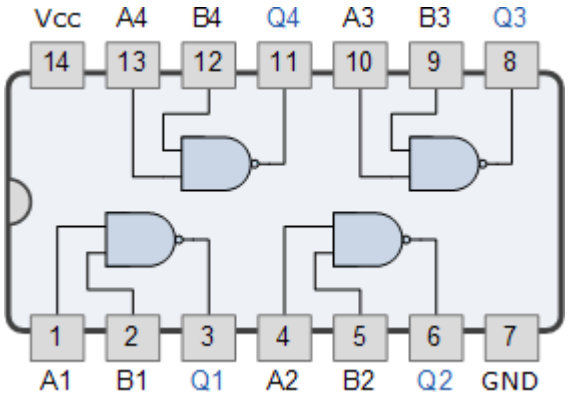
iv) NAND GATE:

SYMBOL:



IC 7400

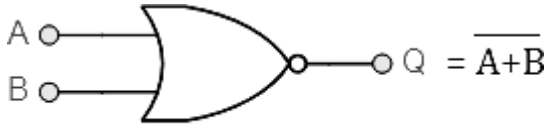
PIN DIAGRAM:



TRUTH TABLE:

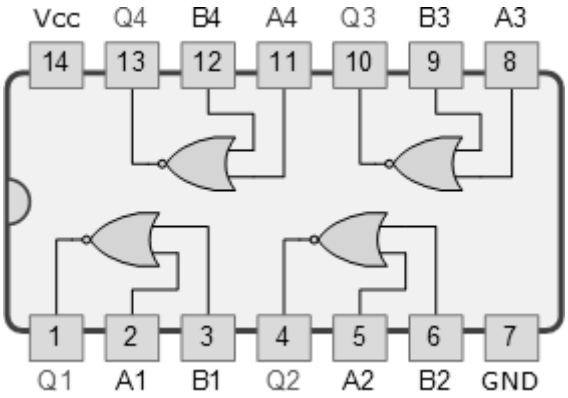
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

v) NOR GATE:
SYMBOL:



IC 7402

PIN DIAGRAM:

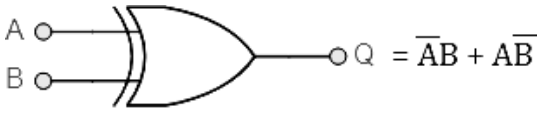


TRUTH TABLE:

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

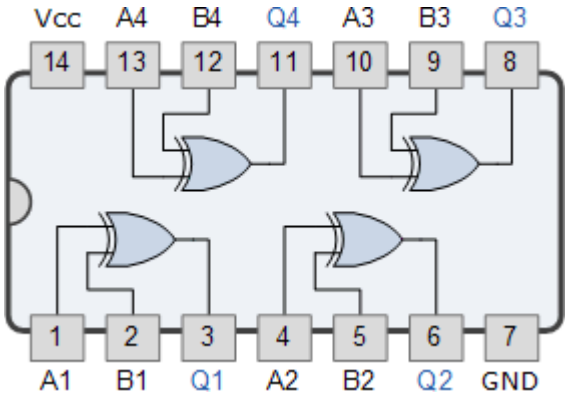
vi) EX-OR GATE:

SYMBOL:



IC 7486

PIN DIAGRAM:

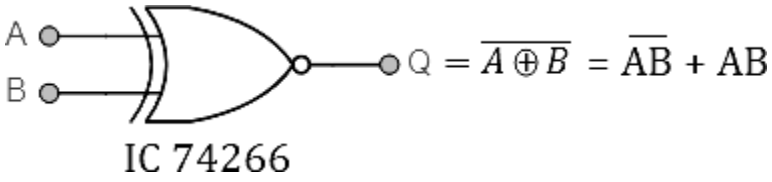


TRUTH TABLE:

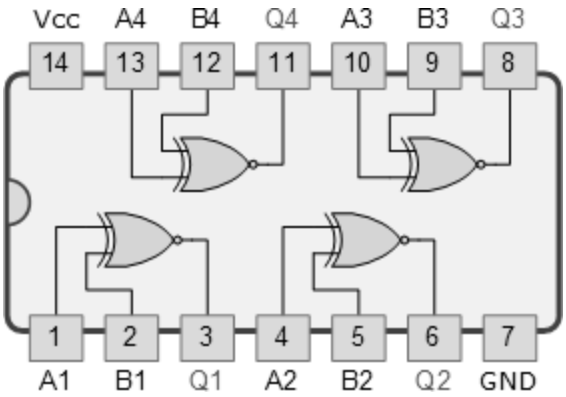
A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

vii) Ex-NOR GATE:

SYMBOL:



PIN DIAGRAM OF IC 74266:



TRUTH TABLE:

A	B	Q =A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

PROCEDURE:

(i) Connect as per pin diagrams (7th pin GROUND & 14th pin Vcc=5V).

(ii) Connect the input to 5V mean logic '1' and connect the input to Ground line mean Logic '0'.

(iii) To observe any output, the output pin to be connect with resistance 1k ohm and LED in series and to be grounded.

(iv) Give the Logical inputs and observe the output & verify the truth table.

Precautions:

- All connections should be made neat and tight.
- ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off
- Never touch live and naked wires.
- Components should be tested before performing the practical.
- When unplugging a power cord, pull on the plug, not on the cable.
- When disassembling a circuit, first remove the source of power.

RESULT:

Thus the truth tables of all basic gates are verified with IC's.

VIVA-VOCE QUESTIONS:

Define gates?

Define IC?

Give example of Demorgan's theorem.

Write the logical equation for AND gate

How many no. of input variables can a NOT Gate have?

Under what conditions the output of a two input AND gate is one?

When will the output of a NAND Gate be 0?

What do you mean by Logic Gates?

What are the applications of Logic Gates?

What is Truth Table?

FLIP FLOPS:S-R, J-K& D	EXPT. NO: 8
	Date:

a) AIM:

To Verify the Truth Tables of S-R, J-K& D flip flops using ICs.

APPARATUS REQUIRED:

i) IC 74LS279,IC 74LS73, IC 7474

ii) LEDs & 1Kohm Resistor

iii) Breadboard

iv) Connecting Wires

THEORY:

A flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

A. R-S flip flop
B. J-K flip flop
C. D flip flop
D. T flip flop

A) RS flip flop

The basic NAND gate RS flip flop circuit is used to store the data and thus provides feedback from both of its outputs again back to its inputs. The RS flip flop actually has three inputs, SET, RESET and clock pulse.

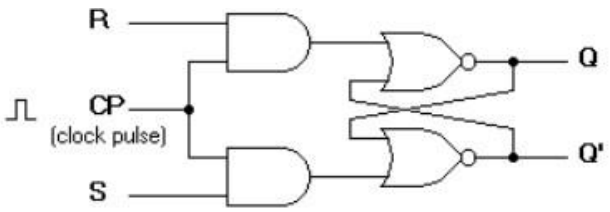


Figure-1:R-S flip flop circuit diagram

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

Figure-2:Characteristics table of R-S flip flop

74LS279 Pinout Diagram

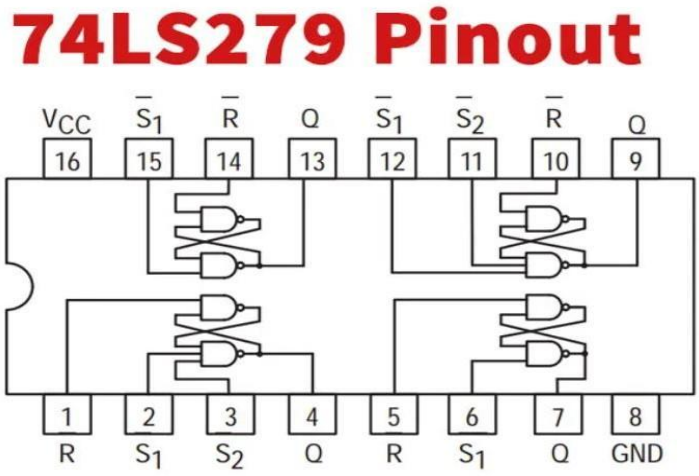


Fig.2a.pin diagram of SR FLIP FLOP

74LS279 Pin Description

Pin No	Pin Name	Description
1	R	Reset Pin
2	S1	Set Pin 1 Of Latch 1
3	S2	Set Pin 2 Of Latch 1
4	Q	Output Of Latch 1
5	R	Reset Pin
6	S1	Set Pin 1 Of Latch 2
7	Q	Output Of Latch 2
8	GND	Ground Pin
9	Q	Output Of Latch 3
10	R'	Reset Pin(Active Low)
11	S'2	Set Pin(Active Low) of Latch 3
12	S'1	Set Pin(Active Low) of Latch 3
13	Q	Output Of Latch 4
14	R'	Reset Pin(Active Low)
15	S'1	Set Pin(Active Low) of Latch 4
14	VCC	Positive Supply

Fig.2b: pin description table for SR flip flop

B:J-K flip flop

In a RS flip-flop the input R=S=1 leads to an indeterminate output. The RS flip-flop circuit may be re-joined if both inputs are 1 than also the outputs are complement of each other as shown in characteristics table below.

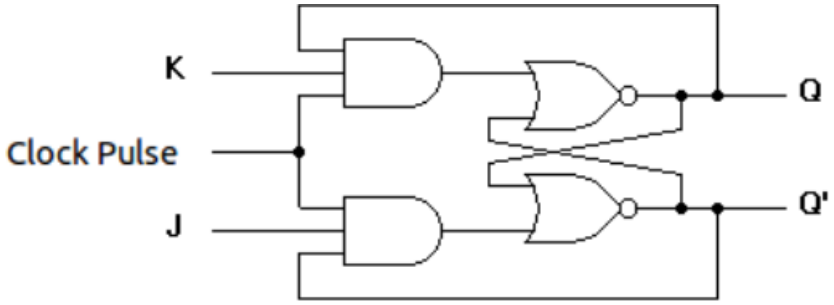


Figure-3:Circuit diagram of J-K flip flop

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
⊠	x	x	-		-		Latched
⊓	0	0	0	1	0	1	No Change
⊓			1	0	1	0	
⊓	0	1	0	1	0	1	Reset
⊓			1	0	0	1	
⊓	1	0	0	1	1	0	Set
⊓			1	0	1	0	
⊓	1	1	0	1	1	0	Toggles
⊓			1	0	0	1	

Figure-4:Characteristics table of J-K flip flop

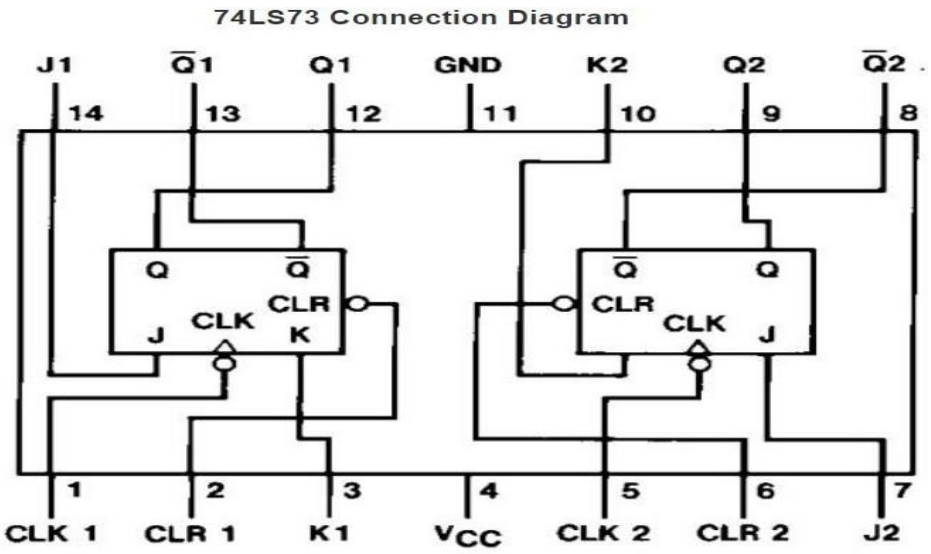


Fig.4a. pin diagram of JK FLIP FLOP

Pin No	Pin Name	Description
1	CLK1	Clock input pin 1
2	CLR1—	Active low clear pin 1
3	K1	Input pin K1
4	VCC	Supply Voltage
5	CLK2	Clock input pin 2
6	CLR2—	Active low clear pin 2
7	J2	Input pin J2
8	Q2—	Active low output 2 pin
9	Q2	Active high output 2 pin
10	K2	Input pin K2
11	GND	Ground Pin
12	Q1	Active high output 1 pin
13	Q1—	Active low output 1 pin
14	J1	Input pin J1

Fig.4b: pin description table for JK flip flop

C:D flip flop

A D flip flop has a single data input. This type of flip flop is obtained from the SR flip flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked SR flip-flop is known as D-flip-flop and is shown below. From the truth table of SR flip-flop we see that the output of the SR flip-flop is in unpredictable state when the inputs are same and high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

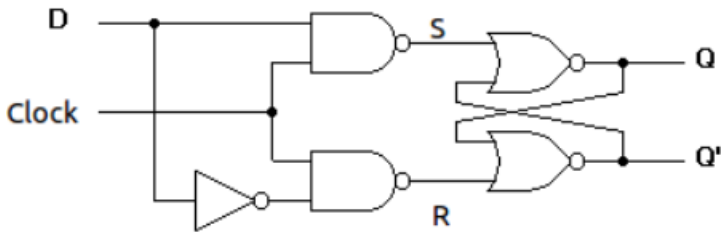


Figure-5:Circuit diagram of D flip flop

Input			Output	
D	reset	clock	Q	Q'
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Figure-6:Characteristics table of D flip flop

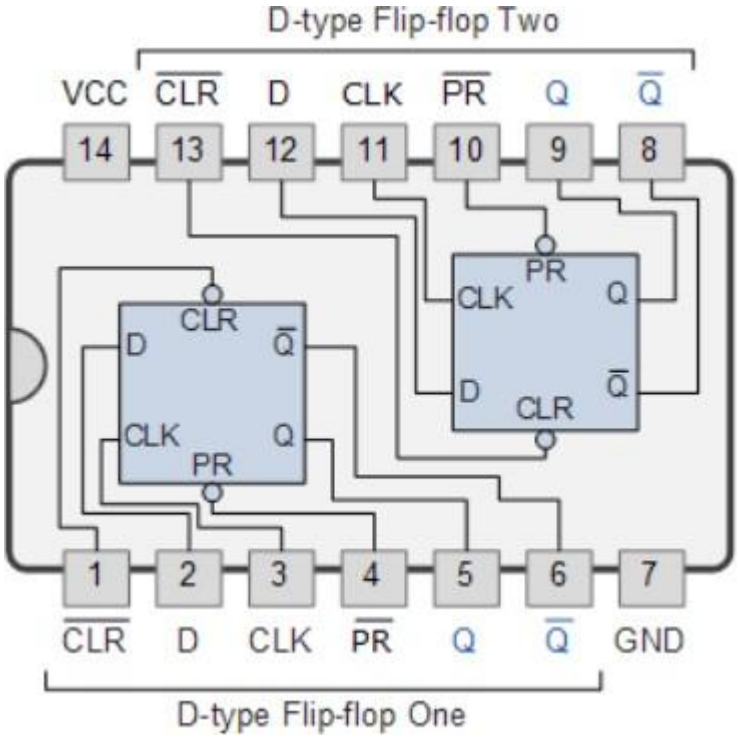


Fig.6a. pin diagram of IC 74LS74 D FLIP FLOP

74LS74 Pin Description

Pin No	Pin Name	Description
1	1CLR’	Resets the flip flop by clearing its memory
2	1D	Input pin of the Flip Flop
3	CLK1	Clock pin for 1st flip-flop
4	1SET’	Input SET pin for flip-flop
5	1Q	Output Pin of the Flip Flop
6	1Q’	The inverted output pin of Flip Flop
7	GND	Ground
8	2Q’	The inverted output pin of Flip Flop
9	2Q	Output Pin of the Flip Flop
10	2SET’	Input SET pin for flip-flop
11	2CLK	Clock pin for 2nd flip-flop
12	2D	Input pin of the Flip Flop
13	2CLR’	Resets the flip flop by clearing its memory
14	VCC	Supply Voltage

Fig.6b. pin description of D FLIP FLOP

PROCEDURE:

A) SR FLIP FLOP

i. Connect pin diagram as shown in fig.2a as per given pin description Fig.2b..

ii. The Logical inputs are given for all the possible combinations.

iii. Observe the output and verify the truth table.

B) JK FLIP FLOP

i. Connect pin diagram as shown in fig.4a as per given pin description fig.4b.

ii. The Logical inputs are given for all the possible combinations.

iii. Observe the output and verify the truth table.

C) D FLIP FLOP

i. Connect pin diagram as shown in fig.6a as per given pin description fig.6b.

ii. The Logical inputs are given for all the possible combinations.

iii. Observe the output and verify the truth table.

Precautions:

- All connections should be made neat and tight.
- ICs should be handled with utmost care.
- While making connections main voltage should be kept switched off
- Never touch live and naked wires.
- Components should be tested before performing the practical.
- When unplugging a power cord, pull on the plug, not on the cable.
- When disassembling a circuit, first remove the source of power.

RESULT:

The truth tables of SR,J-K & D flip-flop are verified


BLOCK-II
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